

WILDSTAR™ Clock Synchronization Distribution Board

Reference Manual

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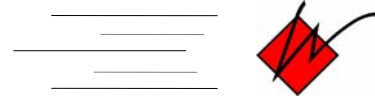
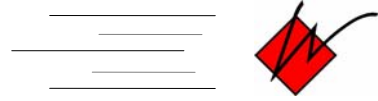


Table of Contents

1	ABOUT THIS MANUAL.....	1-1
1.1	Chapter Overview.....	1-1
1.2	Icons.....	1-2
1.3	Conventions.....	1-3
1.4	Key Words and Definitions.....	1-4
2	INTRODUCTION.....	2-1
2.1	Overview.....	2-1
2.2	Features.....	2-1
3	INSTALLING THE A/D CLOCK SYNCH DISTRIBUTION BOARD.....	3-1
3.1	Unpacking the Board.....	3-1
3.2	Board Installation.....	3-1
3.3	Switches.....	3-3
3.3.1	Front Panel Switch: Input Source Selection.....	3-5
3.3.2	Dip Switches.....	3-6
3.3.3	Output Level Switches.....	3-10
3.4	Cables and Connectors.....	3-12
4	OPERATING THE A/D CLOCK SYNCH DISTRIBUTION BOARD.....	4-1
4.1	Inputs.....	4-1
4.1.1	Clock Inputs.....	4-1
4.1.2	External Trigger Input and Trigger Pushbutton.....	4-4
4.2	Outputs.....	4-5
4.2.1	Observing the outputs with an oscilloscope.....	4-5
4.2.2	Driving an Annapolis Micro Systems, Inc. A/D I/O Card.....	4-5
4.2.3	Cascading A/D Clock Synch Distribution Boards.....	4-7
4.2.4	Driving a Third-Party Card.....	4-8
5	HARDWARE SPECIFICATIONS.....	5-1
5.1	A/D Clock Synch Distribution Board Hardware.....	5-1
5.2	General Specifications.....	5-1
5.2.1	Board Physical Specifications and Operating Range.....	5-1
5.2.2	Heat Specifications and Advisory.....	5-1
5.3	Electrical Specifications.....	5-2
5.3.1	Inputs.....	5-2
5.3.2	Outputs.....	5-6
6	TECHNICAL SUPPORT.....	6-1





1 ABOUT THIS MANUAL




This manual provides guidance for the proper installation and use of the WILDSTAR™ Clock Synchronization Distribution board.

1.1 Chapter Overview

- Chapter 1, “**About This Manual**,” outlines the conventions, icons, and key words used throughout the manual.
- Chapter 2, “**Introduction**,” discusses the board’s architecture and performance features.
- Chapter 3, “**Installation**,” describes how to properly unpack and install the WILDSTAR™ Clock Synchronization Distribution board. Switch settings used to configure the board for the desired operation are also discussed, as well as cable requirements.
- Chapter 4, “**Operating the A/D Clock Synch Distribution Board**,” discusses input, output, and configuration requirements when operating the WILDSTAR™ Clock Synchronization Distribution board with other cards or with test equipment.
- Chapter 5, “**Hardware Specifications**,” includes physical and electrical specifications of the board.
- Chapter 6, “**Technical Support**,” provides information for contacting the Annapolis Micro Systems, Inc. Technical Support team.

1.2 Icons

Throughout the manual, important information is highlighted with icons:

Icon	Description
	Information Notes call attention to important features or instructions.
	Cautions are directions that must be followed in order to avoid loss of system data and/or damage to hardware.
	Warnings are directions that must be followed to ensure personal safety.

1.3 Conventions

INFORMATION NOTE

When boards are referred to in this document, the following abbreviations are used:

- **“Distribution Board”** or **“Clock Distribution Board”** stands for all revisions of the WILDSTAR™ Clock Synchronization Distribution board, unless specifically indicated otherwise.
- **“1.5 GHz A/D I/O card”** stands for all revisions of the WILDSTAR™ 1.5 GHz Analog-to-Digital Converter I/O Daughter card.
- **“1.5 GHz PRO A/D I/O card”** stands for all revisions of the WILDSTAR™ 1.5GHz Pro Analog-to-Digital Converter I/O Daughter card, unless specifically indicated otherwise.
- **“Dual GHz A/D I/O card”** stands for all revisions of the WILDSTAR™ Dual GHz Analog-to-Digital Converter I/O Daughter card, unless specifically indicated otherwise.
- **“Dual 1.5 GHz D/A I/O card”** stands for all revisions of the WILDSTAR™ Dual 1.5GHz Digital-to-Analog Converter I/O Daughter card, unless specifically indicated otherwise.
- **“105 MHz A/D I/O card”** stands for all revisions of the WILDSTAR™ 105 MHz Analog-to-Digital Converter I/O Daughter card.
- **“Quad 105 MHz A/D PRO I/O card”** stands for all revisions of the WILDSTAR™ Quad 105 MHz Analog-to-Digital Converter I/O Daughter card.
- **“A/D I/O cards”** stands for the set of all Analog-to-Digital converter I/O Daughter cards offered by Annapolis Micro Systems listed above.

i

1.4 Key Words and Definitions

Some of the terms used throughout the manual are defined below.

A/D

Analog to Digital. The A/D Clock Synch Distribution Board is so named because it is used to synchronize data collection on multiple Analog-to-Digital-Converter (ADC) cards.

LVC MOS

Low-Voltage Complimentary Metal-Oxide Semiconductor.

LVDS

Low-Voltage Differential Signaling.

LVPECL

Low-Voltage Positive Emitter Coupled Logic.

PECL

Positive Emitter Coupled Logic. A differential signaling standard, sometimes more specifically defined in this manual as LVPECL.

QMA Connector

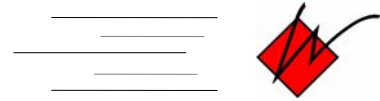
A Quick Mate version of the SMA connector with a snap-on, rather than threaded, interface for more convenient connection and disconnection.

SMA Connector

(Sub-Miniature version A) A threaded coaxial RF connector used for inputs and outputs on the board.

VME

Versa Module Europa. A bus system using the Eurocard standard.



2 INTRODUCTION

2.1 Overview

The Clock Synch Distribution board supplies eight low-skew differential clock outputs and nine low-skew and clock-synchronized, single-ended control signals. These high-speed, low-jitter outputs are ideal for distributing a common clock and synchronized control signal to multiple cards in a system. The control signal is used as a trigger to synchronize data capture on several types of A/D I/O cards available from Annapolis Micro Systems, Inc.

The Clock Distribution board provides the following clock sourcing options for distribution to other cards:

- Single-ended or differential inputs from an external source can be sent into the clock distribution board and forwarded to other cards out the front panel connectors.
- Two on-board oscillators can generate clock signals and distribute them to other cards out the front panel connectors.

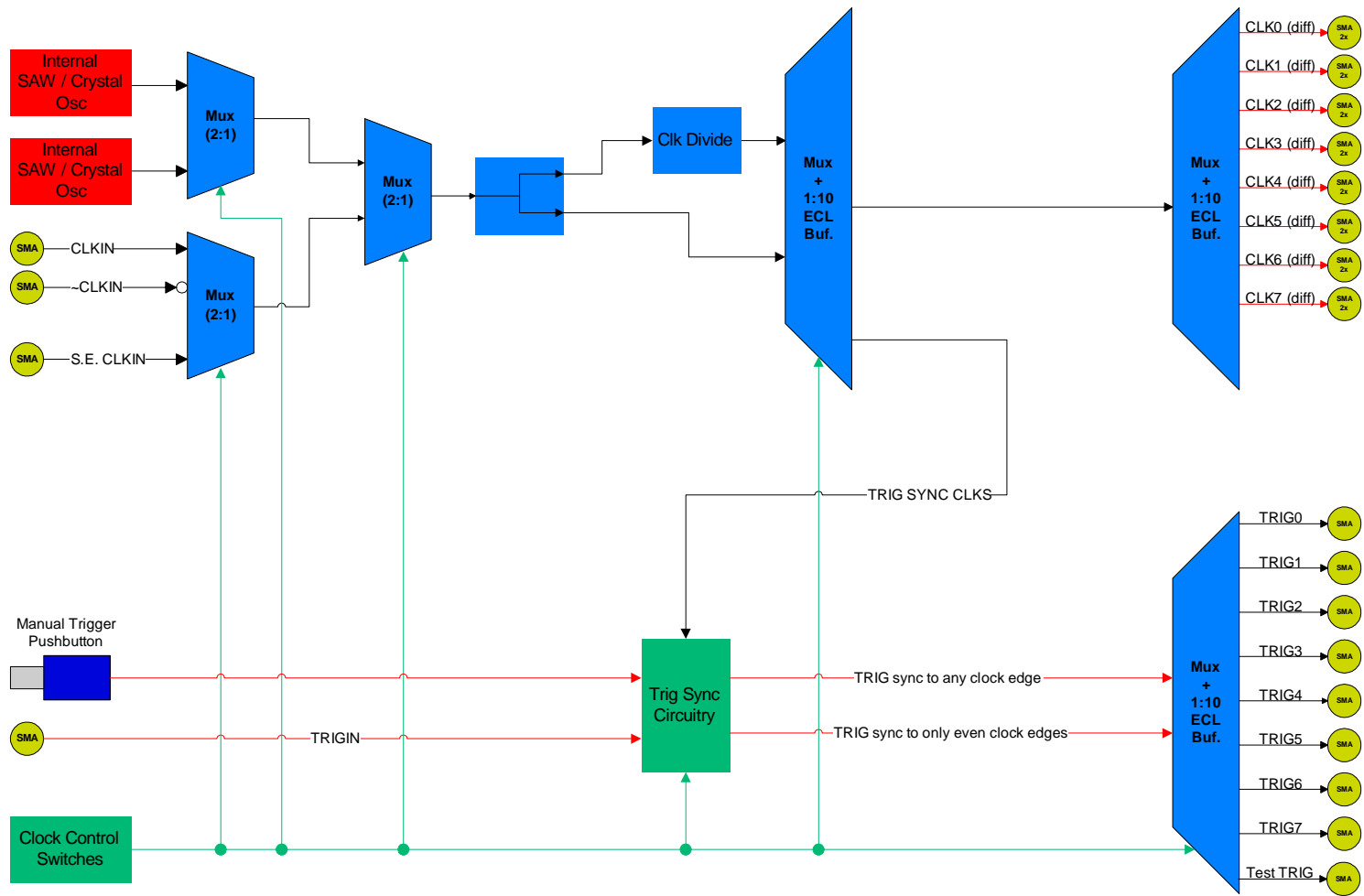
Clock source signals passing through the distribution board or originating on the board itself can be divided for additional frequencies and duty-cycle correction prior to distribution. The nine control trigger outputs can originate from an external source or be generated by a manual pushbutton on the distribution board front panel. These trigger outputs are synchronized to the distributed clock using one of two trigger synchronization modes.

2.2 Features

The Clock Synch Distribution board includes the following features:

- Eight differential clock and nine trigger outputs per board. Boards can be cascaded to provide 64 sets of outputs.
- Compatible with standard VME or VME64X 6U backplanes.
- Requires only +5V and -12V power from backplane.
- Single-Ended clock input supports wide range of signal options, including signal generator sine wave.
- Differential clock input permits multiple standards: LVDS, 3.3V PECL, 2.5V PECL, and 1.65V PECL.

- Selectable output levels of 3.3V PECL, 2.5V PECL, or 1.65V PECL.
(When in 1.65V mode, outputs can only be connected to a 50Ω-to-GND load, such as an oscilloscope.)
- Compatible with all Annapolis Micro Systems, Inc. A/D I/O cards.
- SMA or QMA connector options for all I/O.
- Supports a broad clock frequency range : 0 - 3GHz
- Ultra-low skew outputs
- Ultra-low clock jitter
- On-board clock oscillators provide fixed frequencies of 100 MHz, 2488 MHz, and other custom frequencies.
- Optional divide-by-two circuit provides additional frequency options and clock duty-cycle correction. Rev. D cards add the ability to divide the clock by four, eight, or sixteen.
- Trigger outputs are synchronized to the output clock. Alternatively they can be synchronized to every other rising edge of the output clock.
- Trigger can be provided from an external source with multiple input level options, or manually from a pushbutton on the front panel.



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Figure 2-1: Clock Synch Distribution Board Block Diagram

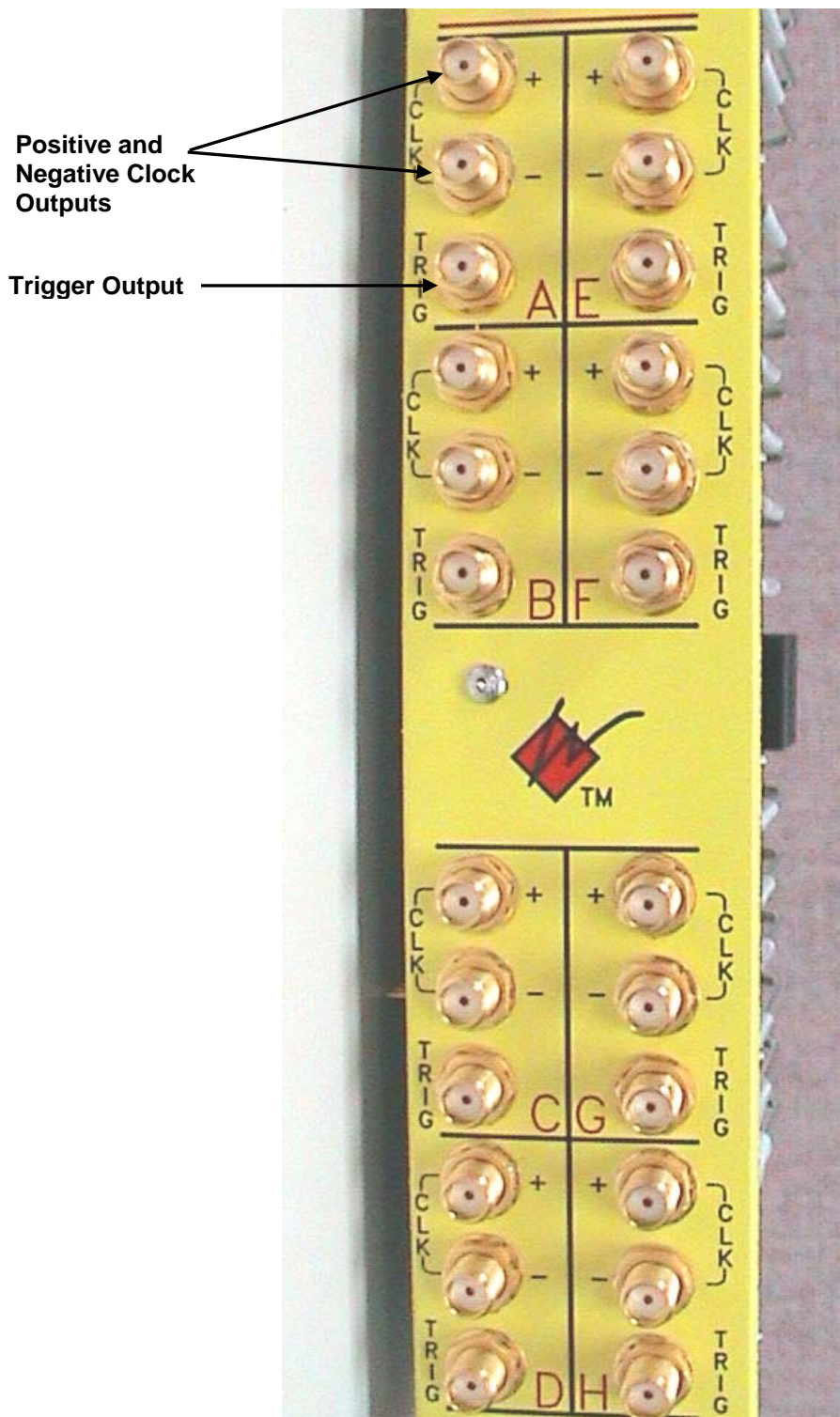
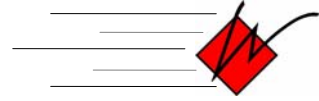


Figure 2-3: Front Panel, showing Clock/Trigger Outputs (detail)





3 INSTALLATION

3.1 Unpacking the Board

The Clock Synch Distribution board is shipped in a static-sensitive pack. The board should remain sealed in this pack until installation time.



CAUTION

Before removing the board from the static pack, ensure that you are properly grounded against static electricity. Use of a ground strap for this purpose is highly recommended, since static discharge to the board could damage its sensitive components.

3.2 Board Installation

1. Connect a ground strap to yourself before handling the board.
2. Shut down the host system and POWER OFF.
3. Hold the board by the front panel ejectors with the VME chassis connectors facing away from the user. The Clock Synch Distribution board occupies two successive slots in a 6U standard VME or VME64X chassis.
4. Gently slide the board into the slot with the board oriented such that the red front panel configuration switch is at the top of the panel.



CAUTION

The Clock Distribution board must be inserted gently into the chassis to avoid damaging the heat sink, cables, or other board components. Be particularly aware of components on the solder side of the board, which have little clearance as the board is inserted.

5. When the VME connectors first contact the backplane connectors, give a firm push on the front panel ejectors. Engage the ejector tabs with the chassis rails to fully seat the board in the VME backplane.



CAUTION

Avoid applying signals to the Clock Distribution board's inputs while the board is not powered. Doing so may damage the board's input circuitry.



CAUTION

Do not connect the Clock Distribution board outputs to an oscilloscope, terminators, or any other device terminated to Ground unless the output is using the 1.65V VCC option. See section 3.3.3.

After the board is properly seated in the chassis, power on the host system.

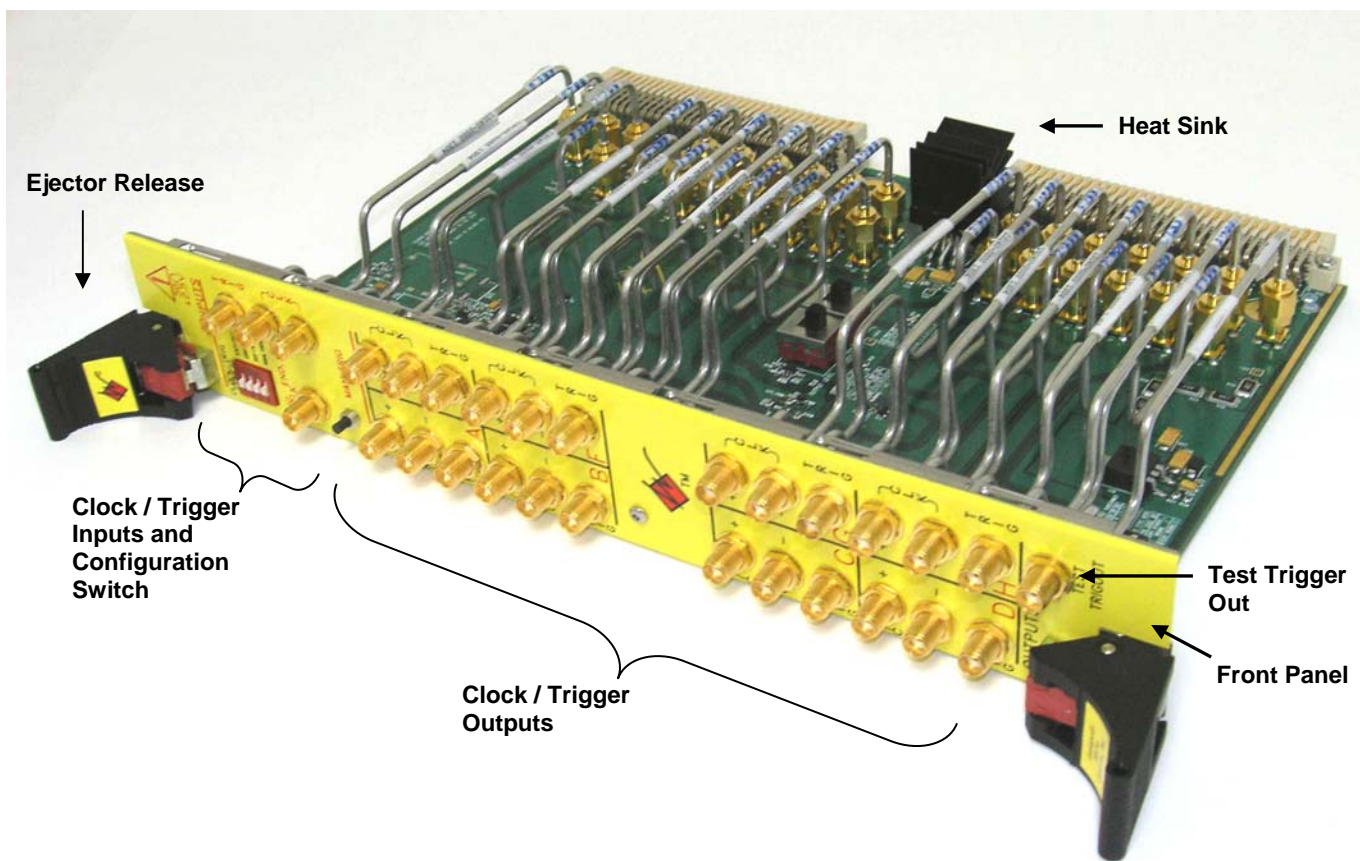


Figure 3-1: Component side front panel view of the Clock Synch Distribution Board

3.3 Switches

All of the Clock Synch Distribution board's clocking and trigger configurations are controlled via four or five sets of switches. Their functions are summarized below and described in more detail in the following sections.

Switch	Function
Front Panel Switch	Selects the clock and trigger input sources
Dip Switch 3 : Trigger Input Options	Controls the input voltage threshold of the external trigger and offers a trigger synchronization mode
Dip Switch 4 : Clock Input Options	Controls the logic level of the external differential clock input and, on Rev C cards, provides the option for divide-by-two duty cycle correction
Dip Switch 7 (Rev D only) : Clock Input Division	Provides the options of dividing the input clock by two, four, eight or sixteen.
Output Level Switches	Control the logic levels of the clock and trigger outputs

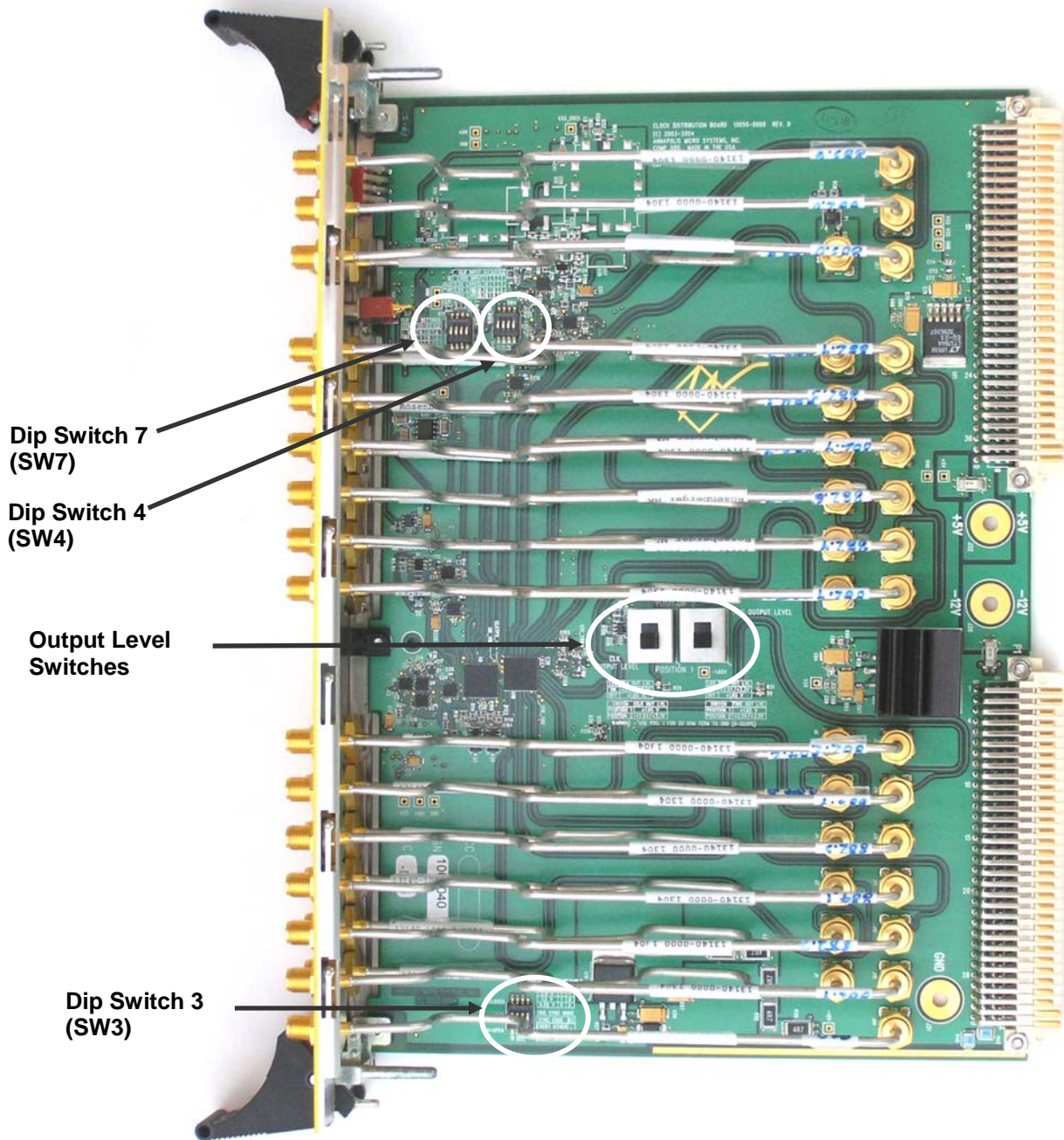


Figure 3-2: Clock Synch Distribution Board Switch Locations. Front panel switch not shown in this view.

3.3.1 Front Panel Switch: Input Source Selection

The sources of clock and trigger inputs for the Clock Distribution board are determined by the four positions of the switch located on the front panel (see Figure 3-3). The switch positions are numbered 1 through 4 from top to bottom and labeled on the front panel. Switch settings are described in the following table and also detailed in the block diagram of Figure 2-1.

Table 3-1: Clock and Trigger Input Source Switch Settings—Front Panel

Switch Position Number and Panel Name	SW OFF	SW ON
Position 1 (EXT/INT)	External Clock	Internal Clock (Oscillator)
Position 2 (OSC 0/1)	Internal Oscillator 0	Internal Oscillator 1
Position 3 (DIF/S.E.)	Differential External Clock	Single-Ended External Clock
Position 4 (MAN. TRIG)	External Trigger Input	Manual Pushbutton Trigger

Position 1 determines whether the clock will be derived from an external source driving Front Panel connector inputs or from one of two internal, on-board oscillators. When the Internal Clock option is selected, **position 2** is used to determine which of two on-board oscillators provides the clock. When the External Clock option is selected, **position 3** determines whether the Single-Ended External Clock input or the Differential External Clock inputs will be used.



CAUTION

When the Single-Ended External Clock is selected as the clock input source but no signal is applied to that input, the clock outputs are likely to toggle at a high rate (2-3GHz) while the board is powered. To avoid these oscillations at the outputs (or the effects of them on the on-board oscillator sources), it is recommended that **position 3** be set to the single-ended external clock only when a signal is being applied to the single-ended clock input.

When **position 4** is set to Manual Pushbutton Trigger (ON), the trigger outputs are controlled by pressing the Manual Trigger button on the board's front panel. The synchronized trigger outputs remain high as long as the button is depressed.

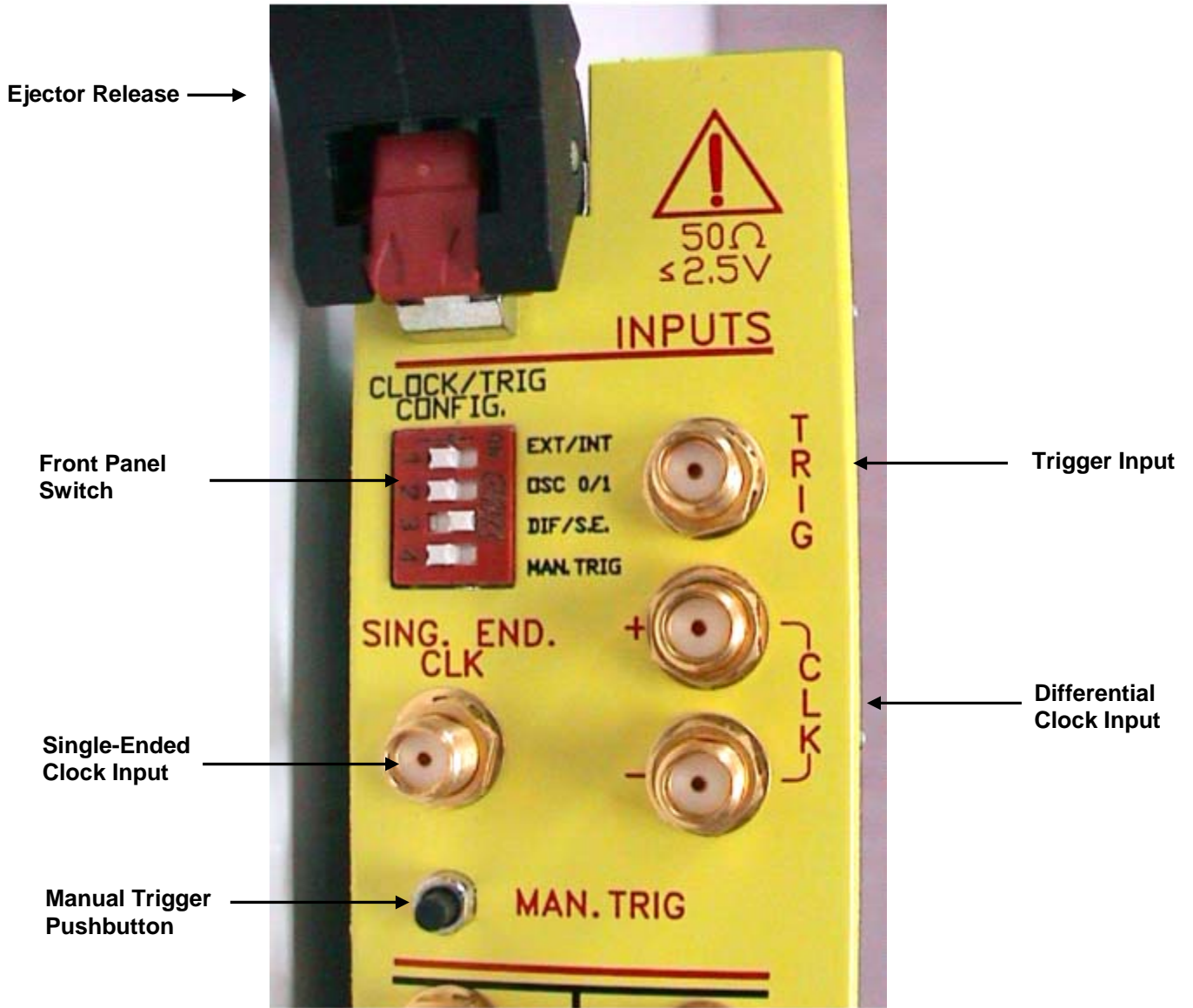


Figure 3-3: Front Panel detail showing clock and trigger inputs and Clock/Trigger Configuration switch

3.3.2 Dip Switches

Two sets of dip switches on the board are used to set clock and trigger input thresholds. These switches are accessible only by removing the board from the chassis.

Dip Switch 3 (SW3): Trigger Input Options

Positions **B1** and **B2** of Dip Switch 3 control the external trigger switching threshold (see Figure 3-4). **Position B3** controls whether the trigger is synchronized to each rising edge or every other rising edge of the clock. Synchronizing the trigger to every other rising edge of the distributed clock is necessary in some applications using the Precision Trigger input of the 1.5GHz Analog-to-Digital Converter I/O Daughter card.

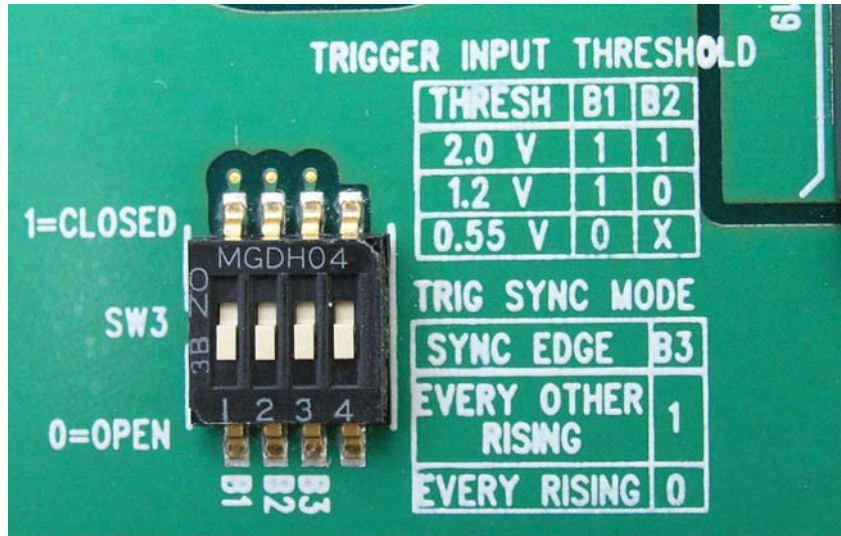


Figure 3-4: Dip Switch 3 (detailed view)

Table 3-2: Trigger Input Threshold Settings

Logic Transition Threshold	B1	B2
2.0V (use with 3.3V LVPECL)	1 (ON)	1 (ON)
1.2V (use with 2.5V LVPECL)	1 (ON)	0 (OFF)
0.55V (use with 1.65V LVPECL)	0 (OFF)	X

Table 3-3: Trigger Synchronization Mode

Sync Edge	B3
Synchronize using every other rising edge	1 (ON)
Synchronize using every rising edge	0 (OFF)

Dip Switch 4 (SW4): Clock Input Options

Positions A1, A2, and A3 of Dip Switch 4 control the External Differential Clock Input Logic level. These positions are not relevant when the single-ended clock input or an on-board oscillator is selected as the clock input source.

On Rev C cards, **Position A4** controls whether the clock input is divided by two before being distributed to the outputs and to the trigger synchronization logic. The divide-by-two function provides additional output frequency options and a means of duty cycle correction. This function applies to all clock input sources: the external differential clock, the external single-ended clock, or the internal clock oscillators.

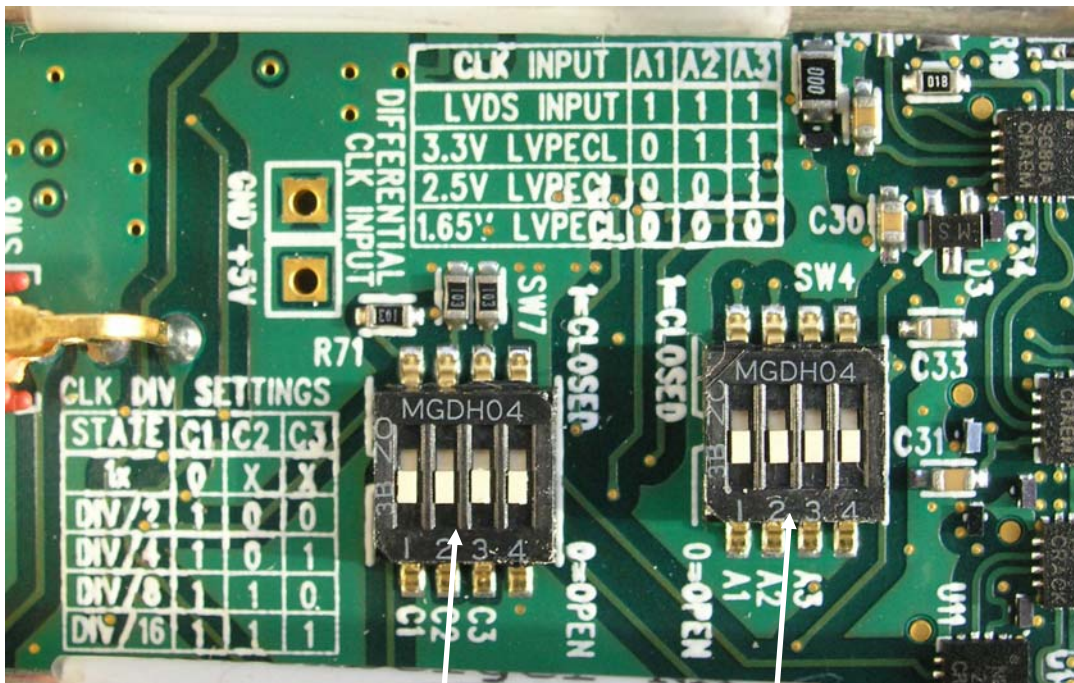


Figure 3-5: Dip Switches 4 and 7 (detailed view)

Table 3-4: External Differential Clock Input Logic Settings

External Differential Clock Input Logic Level	A1	A2	A3
LVDS	1 (ON)	1 (ON)	1 (ON)
3.3V LVPECL	0 (OFF)	1 (ON)	1 (ON)
2.5V LVPECL	0 (OFF)	0 (OFF)	1 (ON)
1.65V LVPECL	0 (OFF)	0 (OFF)	0 (OFF)

Table 3-5: Clock Division / Duty Cycle Correction Setting (Rev C cards only)

Clock Divided by 2	A4
ON	1 (ON)
OFF	0 (OFF)

Dip Switch 7 (SW7): Clock Input Division (Rev D cards)

On Rev D boards, Dip Switch 7 offers the ability to divide the clock input frequency by two, four, eight, or sixteen, before it is distributed to the outputs and to the trigger synchronization logic. Clock division can be used for duty-cycle correction and to produce additional output frequency options. Note that when clock division is enabled, the trigger synchronization is performed using the divided clock.

Table 3-6: Clock Division (Rev D cards only)

Clock Division	C1	C2	C3
÷1 (no division)	0 (OFF)	X	X
÷2	1 (ON)	0 (OFF)	0 (OFF)
÷4	1 (ON)	0 (OFF)	1 (ON)
÷8	1 (ON)	1 (ON)	0 (OFF)
÷16	1 (ON)	1 (ON)	1 (ON)

3.3.3 Output Level Switches

Two large two-position switches on the Clock Synch Distribution board (Figure 3-6) determine voltage options for the clock and trigger outputs. These switches, labeled “CLK OUTPUT LEVEL” and “TRIG OUTPUT LEVEL” (“CLKPWR” and “TRIGPWR” on Rev C cards), are located near the center of the board and can be accessed only by removing the board from the chassis.

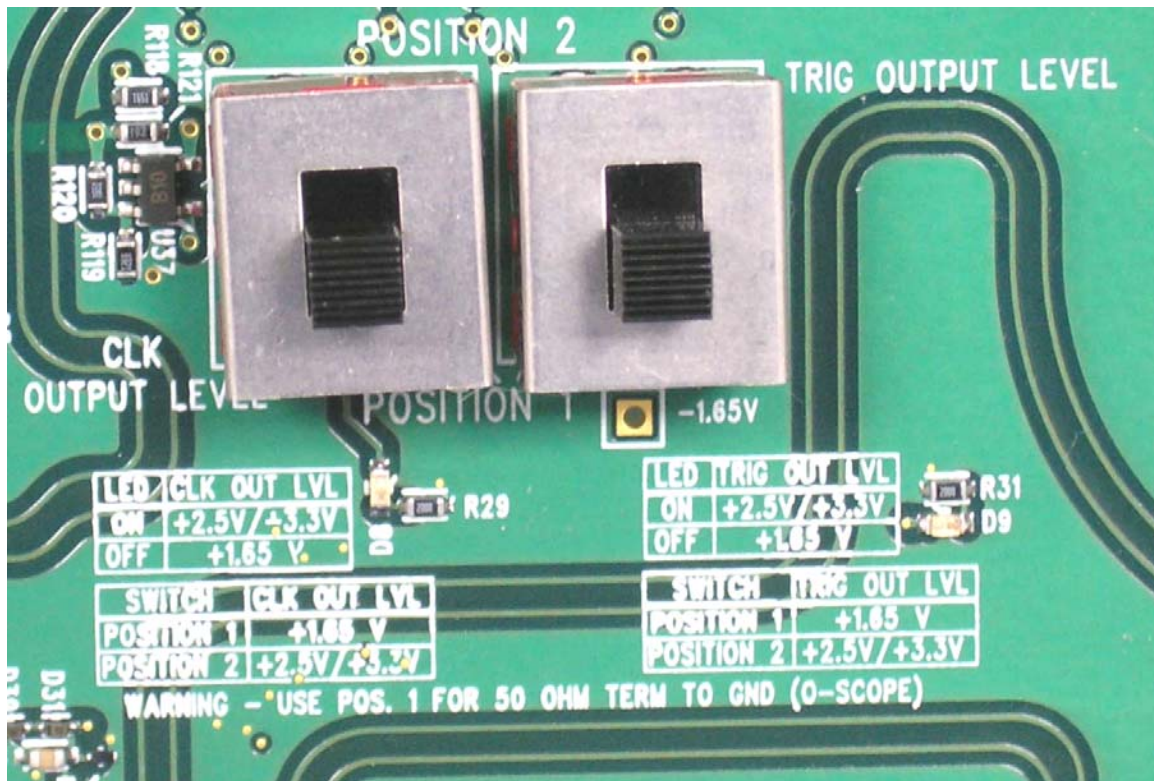


Figure 3-6: Output Level Switches for the Clock (left, facing) and Trigger (right)

Table 3-7: Clock Output Level Switch Settings

CLK OUTPUT LEVEL (CLKPWR)	Position 1	Position 2
		+1.65V PECL

Table 3-8: Trigger Output Level Switch Settings

TRIG OUTPUT LEVEL (TRIGPWR)	Position 1	Position 2
		+1.65V PECL

For both switches, the down position labeled POSITION 1 is required when the clocks or triggers are being driven into an oscilloscope or other device terminated with 50 Ω to ground. The up position, POSITION 2, is used when the clock or triggers are driven to a device terminated with 50 Ω to an elevated voltage (i.e., triggers driven into a 1.5 GHz A/D I/O card).

Whether POSITION 2 represents +2.5V or +3.3V is determined by a build option specified when the board is ordered. Typical configurations are 2.5V PECL for the clock outputs and 3.3V PECL for the trigger outputs.

Small green LEDs located just below each of the Output Level switches indicate position status. When an LED is on, the corresponding switch is in the +2.5V PECL /+3.3V PECL position and the corresponding set of outputs (clock or trigger) should **not** be terminated to ground with an oscilloscope, terminator, or other device.

3.4 Cables and Connectors

The inputs and outputs of the Clock Synch Distribution board require cables with either 50 Ω SubMiniature version A (SMA) threaded plugs or 50 Ω QMA snap-on plugs at each end (sold separately).

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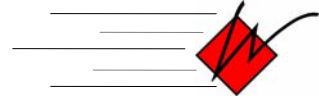
INFORMATION NOTE
To ensure proper contacts at the SMA connectors, make sure the connector plug screws in easily, indicating proper alignment, and tighten until secure. When using a wrench, a torque of 60-100 Ncm is recommended.



Figure 3-7: SMA Cable/Connector End (detail)



Figure 3-8: QMA Cable/Connector End (detail)



4 OPERATING THE CLOCK SYNCH DISTRIBUTION BOARD

4.1 Inputs

This section describes the requirements of drivers of the Clock Synch Distribution board's external clock and trigger inputs.



CAUTION

Avoid applying signals to the Clock Distribution board's inputs while the board is not powered. Doing so may damage the board's input circuitry.



CAUTION

Under no circumstances should the inputs to the Clock Distribution board exceed 2.5V. Consult the Electrical Specifications section for additional restrictions.

4.1.1 Clock Inputs



INFORMATION NOTE

Jitter on the clock outputs is dependent on that of the clock input. To maintain clock outputs with low jitter, a low-jitter input source is required.

Single-Ended Clock Input

AC coupling on the single-ended clock input permits a variety of options for drivers. A sine wave centered about 0V, as from a function generator, is well suited for this input. An input power of +10dBm is typical, which, through a 50 Ω termination corresponds to 707mV, but through the single-ended clock input's 100 Ω termination produces a larger 1V peak-to-peak amplitude.

A broad range of amplitudes and offsets are acceptable on the single-ended clock input, though none should ever exceed +/-2.5V. Refer to the complete specifications for this input in Table 5-3 of the Electrical Specifications.

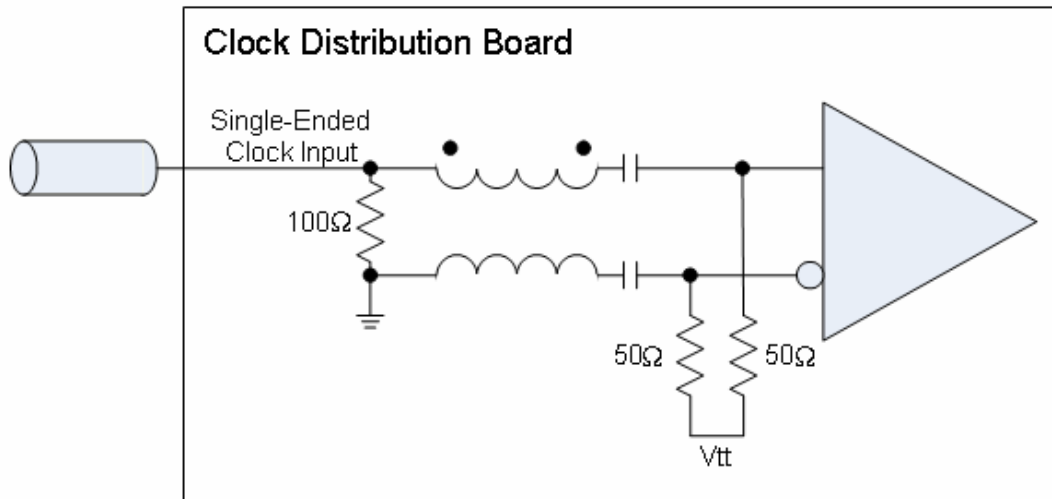


Figure 4-1: Termination of the Single-Ended Clock Input on the Clock Synchron Distribution Board



CAUTION

When the Single-Ended External Clock is selected as the clock input source but no signal is applied to that input, the clock outputs are likely to toggle at a high rate (2-3GHz) while the board is powered. If these output oscillations cannot be tolerated, they can be avoided by selecting the Differential External Clock as the clock source until a signal can be applied to the Signal-Ended Clock input.

Differential Clock Input

Unlike the single-ended clock input, the differential clock input should not be driven by a sine wave generator. Instead, LVPECL and LVDS differential standards are supported.

LVPECL drivers expect termination to specific voltage levels which are ultimately based on the driver's positive supply voltage, V_{cc} . The Distribution Board's differential clock inputs permit LVPECL drivers with three nominal V_{cc} levels: 1.65V, 2.5V, and 3.3V. Matching the differential clock input to the appropriate driver standard is accomplished with Dip Switch 4 (see section 3.3.2).

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INFORMATION NOTE
Though the Clock Distribution Board's differential clock input is intended for LVPECL or LVDS differential drivers, a single-ended driver with an A/C coupled output could be used to drive only one of the Distribution Board's differential clock inputs. In this case, leave the other input open. Do not terminate it.

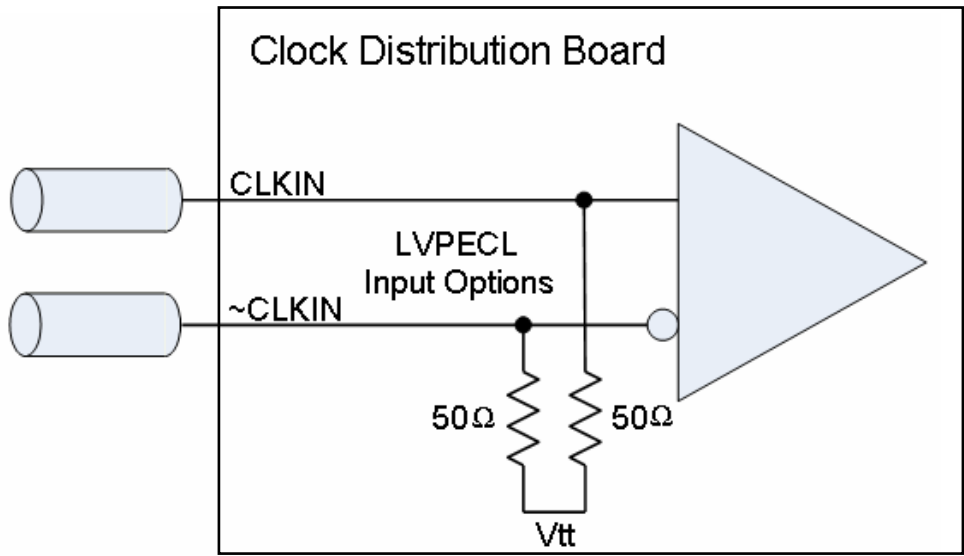


Figure 4-2: LVPECL termination of the differential clock inputs on the A/D Clock Synch Distribution Board. The LVPECL termination and the termination voltage, V_{tt}, are controlled with Dip Switch 4.

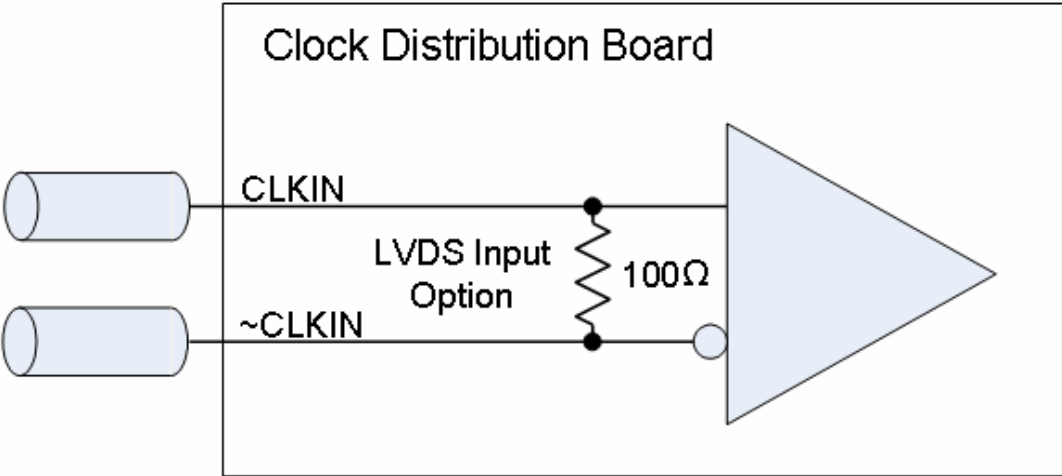


Figure 4-3: LVDS termination of the differential clock inputs on the A/D Clock Synch Distribution Board. LVDS termination can be selected with Dip Switch 4.

4.1.2 External Trigger Input and Trigger Pushbutton

The external trigger input can be configured to detect transitions around three possible positive voltage thresholds (see section 3.3.2). A pulse-generator producing a signal with a positive offset can be used to produce valid inputs as can the single output of a LVPECL differential pair. Other standards such as 2.5V LVCMOS may also be acceptable, provided they are capable of driving the 50 Ω termination (Figure 4-4) while maintaining the required V_{il} and V_{ih} levels. Refer to the trigger input electrical specification in Table 5-4.

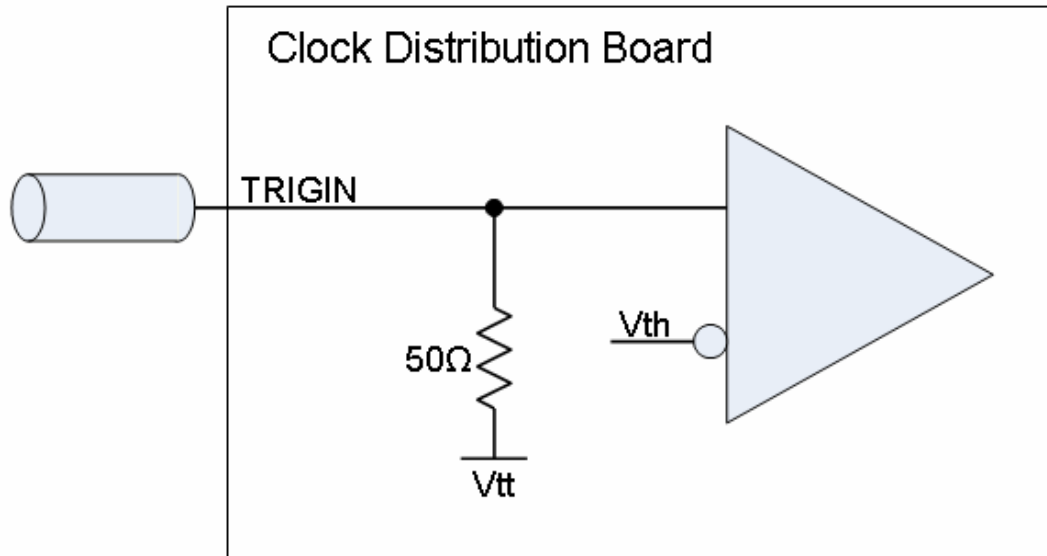


Figure 4-4: Trigger input termination on the Synch Distribution Board. The switching threshold, V_{th} , and termination voltage, V_{tt} , are controlled by Dip Switch 3.

Alternatively, triggers can be generated with the manual trigger pushbutton located on the front panel of the Clock Synch Distribution board. When the pushbutton is chosen as the trigger source, as determined by the front panel switch (section 3.3.1), the external trigger input is bypassed. In this configuration, pressing the manual pushbutton results in a single active-high pulse on the nine trigger outputs. The trigger outputs remain high for as long as the button remains depressed.

Trigger inputs, whether from the connector or pushbutton, are synchronized to the Distribution Board's output clocks such that all trigger output transitions occur together a fixed amount of time following a rising edge of the clock outputs. In the absence of any trigger input, the eight trigger outputs remain at a logic-low level, V_{ol} .

4.2 Outputs

All board outputs are reduced-swing Positive ECL, and are capable of driving oscilloscopes, A/D I/O cards provided by Annapolis Micro Systems, Inc., and other A/D Clock Synch Distribution Boards, as long as the appropriate output levels are chosen. These requirements are discussed in the following sections, along with more specific requirements for driving other devices or other cards provided by a third party.



INFORMATION NOTE

When driving a single-ended clock input with a differential clock output, it is recommended that the unused member of the differential output be terminated in the same manner and, when possible, through the same length cable as the used output.

4.2.1 Observing the outputs with an oscilloscope

Outputs of the Clock Distribution board can be observed on an oscilloscope when the scope provides 50 Ω termination to ground AND the Clock Distribution board's output levels are set to 1.65V (see Section 3.3.3).



CAUTION

Never apply power to the Clock Distribution board when its outputs are terminated to Ground, unless the level of the terminated outputs is first set to 1.65V PECL (see Section 3.3.3).

If the board drives a card requiring an output level other than 1.65V, it should be disconnected from that card before being connected to the oscilloscope to avoid conflicting output requirements.

When viewing clock outputs with an oscilloscope, best results are achieved by terminating both outputs of a differential pair to the scope, or by terminating the unused member of the pair with a matched-length cable to a 50 Ω terminator.

4.2.2 Driving an Annapolis Micro Systems, Inc. A/D I/O Card

Input / Output Levels

A/D I/O cards from Annapolis Micro Systems, Inc. are equipped with the proper input termination for the Clock Distribution board's LVPECL outputs, provided that the Clock Distribution Board is operating with the proper output levels. The

output levels are the chosen by a pair of switches on the board (see Section 3.3.3). Valid Clock Distribution board output levels for each A/D I/O card type are summarized in the table below.

Table 4-1: Distribution Board output settings when driving Annapolis Micro Systems, Inc. A/D I/O cards

	Distribution Board Clock Output Level	Distribution Board Trigger Output Level
1.5GHz A/D I/O Card	1.65V PECL	3.3V PECL**
1.5GHz Pro A/D I/O Card	1.65V PECL	1.65V PECL
Dual GHz A/D I/O Card	1.65V PECL	1.65V PECL
105 MHz A/D I/O Card	1.65V PECL	Not Compatible
Quad 105 MHz A/D I/O Card	1.65V PECL or 2.5V PECL*	1.65V PECL
Dual 1.5GHz D/A I/O Card	1.65V PECL	1.65V PECL

*The proper level depends on the build option of the A/D I/O card.

** The 1.5GHz A/D I/O Card must be built with the “EXTCLKDB” factory option.

INFORMATION NOTE

Annapolis Micro Systems, Inc. A/D I/O Cards with differential clock inputs may require that both positive and negative clock inputs be driven to function properly.

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Timing Requirements / Cable Lengths

The clock and trigger input timing requirements of the 1.5GHz PRO, Dual GHz A/D, Dual 1.5GHz D/A, and Quad 105MHz A/D I/O cards are satisfied when the Clock Distribution board uses delay-matched cables to deliver the clocks and triggers from Distribution board to I/O card.

CAUTION

The required trigger hold time of the Dual GHz and 1.5 GHz PRO cards, however, is just barely met by the Distribution board’s minimum clock-to-output time. A slight difference in the clock and trigger cable propagation delays could result in a violation of this specification. This risk can be minimized by favoring slightly longer cables for the trigger connections.

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INFORMATION NOTE

The best practice is to refer to the trigger output characteristics of the Distribution board (Table 5-9) and to the trigger input requirements of the A/D I/O card, in order to determine the relative clock and trigger cable lengths which yield the greatest possible setup and hold margins for the sample clock period being used.

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The timing requirements of the 1.5GHz A/D I/O card are more complicated than those of the other A/D I/O cards. For one, the trigger setup times are frequency dependent. Recommended cable lengths for a range of input clock frequencies appear in the hardware reference section of the *WILDSTAR™ 1.5 GHz A/D I/O Daughter Card Reference Manual*. In addition, the trigger must only transition on every other rising edge of the clock. This alternative is provided by the Trigger Options Switch (Dip Switch 3) on the Clock Distribution board. Consult the Hardware Reference section of the *WILDSTAR™ 1.5 GHz A/D I/O Daughter Card Reference Manual* for additional requirements of the 1.5 GHz A/D I/O card inputs.

4.2.3 Cascading Clock Synch Distribution Boards

When more than eight outputs are required, or when clock or trigger outputs must drive devices requiring different levels, multiple Clock Distribution boards can be cascaded with one master board driving two to eight slave boards. This configuration requires the considerations listed in the following table.

Table 4-2: Considerations for Driving Multiple Boards with the Distribution Board

	“Master” Board	“Slave” Board
Front Panel Switches	Choose according to the input source	Select the External Differential Clock and the External Trigger Input
Clock Division / Duty Cycle Correction	If duty cycle correction is desired, select it using Dip Switch 7 (Dip Switch 4 on Rev C boards). Note that when duty cycle correction is enabled, the board’s output clock frequency will be a fraction of that of the input clock or clock oscillator	Should be DISABLED in general, since the divide circuit could result in output clocks of different slave boards being out of phase.
Trigger Synchronization	If the trigger is to be synchronized to every other rising clock edge, as when used with a 1.5GHz A/D I/O Card, select this option using Dip Switch 3.	Trigger synchronization to every other rising edge of the clock should be DISABLED since it could cause the output triggers of different slave boards to be synchronized to different clock edges.
Output Levels	Use the Output Level switches to match the input levels of the slave board. For proper operation when cascading boards, the trigger output level is required to be 1.65V.	
Input Levels		Use Dip Switch 4 to match the level of the external Differential clock input to the master board’s clock output. Note that the master board has LVPECL, not LVDS, outputs, so LVDS is not a valid slave board input option. Use Dip Switch 3 to set the trigger input threshold to 0.55V, corresponding to the master’s required trigger output of 1.65V PECL.

i**INFORMATION NOTE**

To maintain low skew and trigger synchronization, the propagation delay through all cables from the master to slave boards should be matched in length.

i**INFORMATION NOTE**

Connect both the positive and negative differential clocks from the master to slave board. Though only one member of each master board's differential clock output pair can be connected to the slave boards' single ended clock inputs, this is not recommended as it degrades performance.

4.2.4 Driving a Third-Party Card

The Clock Distribution board uses reduced-swing Positive ECL type outputs. As such, they expect termination at the receiver consisting of a resistive path to a low-noise termination voltage, V_{tt} . For proper operation, V_{tt} must be lower in potential than the lowest possible V_{ol} .

The line characteristic impedance of the Clock Distribution board outputs is approximately $50\ \Omega$, so for best results, match this impedance with $50\ \Omega$ termination resistors to $V_{tt} = (V_{cc} - 1.5V)$, where V_{cc} is the value selected by the Output Level Switch settings. Note that the termination node, V_{tt} , must be able to sink the current from the Distribution Board's output drivers.

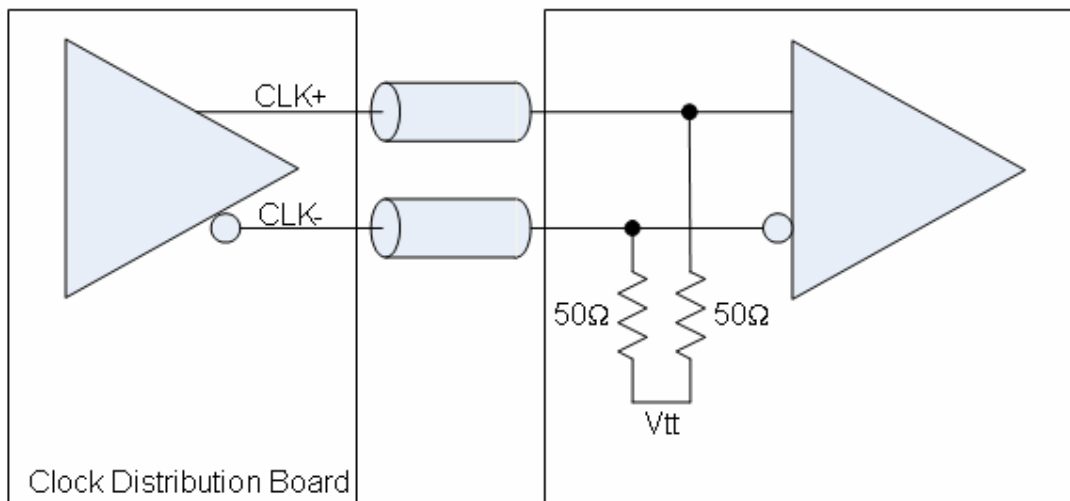


Figure 4-5: Standard termination for the Distribution Clock Outputs

The trigger outputs are distributed as single-ended signals, but have the same termination requirements as the differential clock outputs. If a trigger output is

used to drive a differential input, the unused input needs to be biased to a voltage as close as possible to the trigger's transition threshold. A simple way of accomplishing this is with a resistor divider as shown in Figure 4-6. The resistor values are chosen such that V_{bb} is midway between the V_{oh} and V_{ol} of the trigger output.

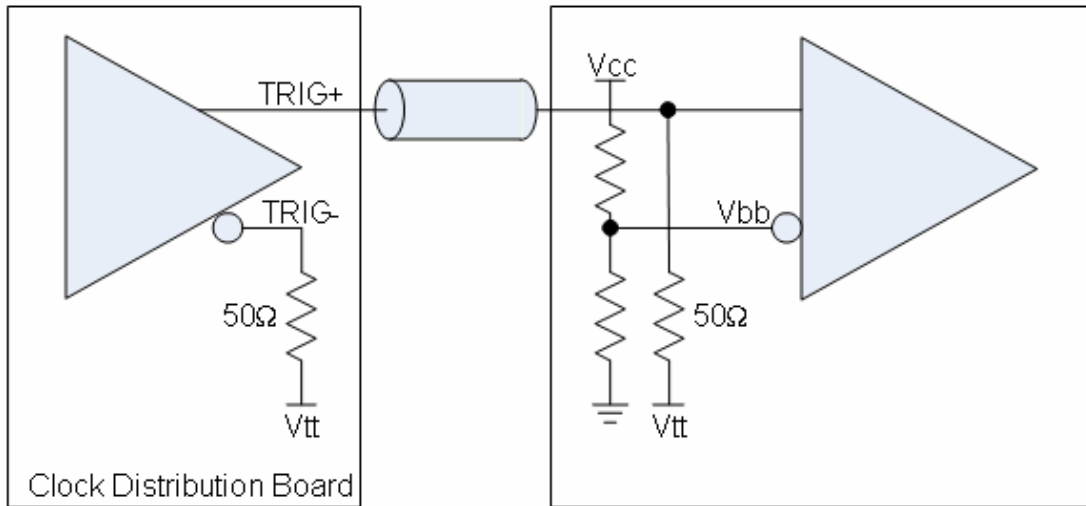


Figure 4-6: Standard termination for the Distribution Trigger Outputs

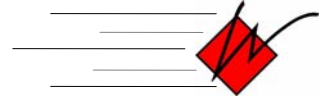
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INFORMATION NOTE

The body, or shell, of the receiver boards' SMA connectors should be electrically connected to the receiver board's ground, regardless of the required termination voltage.

Consult the Electrical Specifications section for complete input and output requirements of the clock and trigger outputs.





5 HARDWARE SPECIFICATIONS

5.1 Clock Synch Distribution Board Hardware

This chapter contains hardware reference information, including physical, electrical, and temperature specifications, for the Clock Synch Distribution board.

5.2 General Specifications

5.2.1 Board Physical Specifications and Operating Range

Table 5-1 specifies the physical dimensions and operating range for the board:

Table 5-1: Clock Synch Distribution Board Specifications

Board Physical Dimensions	Length: 9.19 inches Width: 6.87 inches Thickness: 0.070 inches Assembled Weight: 23 oz.
Front Panel	Faceplate Width: 1.595 inches Connectors: Rosenberger 50 Ω SMA Bulkhead Jacks / 50 Ω QMA Bulkhead Jacks
Operating Range	Temperature: 0° to 70°C

5.2.2 Heat Specifications and Advisory

It is critical that heat limits for the Clock Synch Distribution board be observed. Airflow of at least 25 cfm per VME slot should be maintained. This recommendation should be followed along with ensuring that the heat sink on the board is installed properly.



CAUTION

The Clock Synch Distribution board has a large heat sink to aid in heat dissipation (Figure 3-1). To prevent system damage, fire, and personal injury, never use these boards without the heat sink installed.



INFORMATION NOTE

Cooling may be improved by leaving the adjacent slots of the installed Distribution board unpopulated. This may also reduce the potential effects of EMI radiation on the board.

5.3 Electrical Specifications

5.3.1 Inputs

Table 5-2: Differential Clock Input: CLKIN / ~CLKIN

Characteristic	Minimum	Typical	Maximum	Units
Vih Input High Voltage				
LVDS	400	1450	2500	mV
3.3V LVPECL	1475	2300	2500	
2.5V LVPECL	825	1500	2500	
1.65V LVPECL	400	750	2500	
Vil Input Low Voltage				
LVDS	-800	1050	Vih - 75	mV
3.3V LVPECL	1430	1700	Vih - 75	
2.5V LVPECL	770	900	Vih - 75	
1.65V LVPECL	45	350	Vih - 75	
Vtt-in Termination Voltage				
LVDS	N/A	N/A	N/A	mV
3.3V LVPECL	1310	1350	1390	
2.5V LVPECL	690	710	730	
1.65V LVPECL	0	3	5	
Clock Frequency	0		3000	MHz
Maximum Clock Frequency to maintain synchronous trigger*			1940	MHz

All LVPECL differential clock input configurations are terminated with 50 Ω to the Termination Voltage. The LVDS input configuration is terminated with 100 Ω across the differential pair.

All differential input voltage and input common mode voltage requirements are met by observing Vil and Vih.

* When clock division is enabled, this represents the limit of the divided clock rather than the input clock. Note that in this case, the input clock rate is still constrained by the general Clock Frequency limits.

Table 5-3: Single-Ended Clock Input: S.E. CLKIN

Characteristic	Minimum	Typical	Maximum	Units
Input power				
30-100 MHz	0	15.0	17.9	dBm
100-2000 MHz	-7.5	10.0	17.0	
2000-3000 MHz	-6.5	11.0	17.9	
Input Termination (see Figure 4-1)		50Ω to GND		
Vih			2.5 (Absolute Maximum)	V
Vil	-2.5 (Absolute Minimum)			V
Clock Frequency	30		3000	MHz
Maximum Clock Frequency to maintain synchronous trigger*			1940	MHz

* When clock division is enabled, this represents the limit of the divided clock rather than the input clock. Note that in this case, the input clock rate is still constrained by the general Clock Frequency limits.

Table 5-4: Trigger Input: TRIGIN

Characteristic	Minimum	Typical	Maximum	Units
Vih Input High Voltage Threshold = 550 Threshold = 1200 Threshold = 2000	650 1300 2100		2500 2500 2500	mV
Vil Input Low Voltage Threshold = 550 Threshold = 1200 Threshold = 2000	Greater of -800 and (Vih - 2600)		450 1100 1900	mV
Vtt-in Termination Voltage Threshold = 550 Threshold = 1200 Threshold = 2000	0 670 1285	2 690 1325	5 710 1370	mV
External Trigger to Rising Edge of Differential Clock Setup*	285			ps
External Trigger to Rising Edge of Differential Clock Hold*	-125			ps

* External Trigger to Single-Ended Clock setup and hold times are unpublished because they are frequency dependent. Regardless of the clock source, the trigger is synchronized through a series of registers, virtually guaranteeing no metastability problems when setup or hold times are violated. However, to maintain trigger synchronization across multiple Clock Distribution boards in a cascaded configuration, the downstream slave boards must employ their differential clock inputs and meet these specified trigger setup and hold requirements.

Note that the TRIGIN trigger input is terminated to the Termination Voltage through a 50 Ω resistor (see Figure 4-4). The driver must be capable of sourcing the current required by this termination. If the driver is series terminated, driver output levels will be divided at the trigger input.

Table 5-5: Power Characteristics

Characteristic	Minimum	Typical	Maximum	Units
5V supply current: Static – External clock input, no outputs terminated		1550		mA
100MHz on-board clock oscillator, no outputs terminated		1575		
2.448GHz on-board clock oscillator, no outputs terminated		1675		
Additional current per terminated output		11		
-12V supply current: 1.65V LVPECL clock and trigger outputs		180		mA
2.5V/3.3V LVPECL clock and trigger outputs		10		

*5V supply current values can increase slightly with temperature, but remain essentially constant over all clock frequencies.

5.3.2 Outputs

Below are tables showing clock and trigger output details for the Clock Distribution board.

Table 5-6: Clock Outputs

Characteristic	Minimum	Typical	Maximum	Units
Voh Output High Voltage				
CLK Output Level 3.3V	2270	2330	2380	mV
CLK Output Level 2.5V	1500	1560	1610	
CLK Output Level 1.65V	640	700	750	
Voutpp Output Voltage Amplitude*	300	370	450	mV
Vtt-out Termination Voltage**				
CLK Output Level 3.3V	1295	1500	1800	mV
CLK Output Level 2.5V	495	750	1010	
CLK Output Level 1.65V	-355	0	150	
Iout Output Current				
Continuous			25	mA
Surge			50	
Clock output to output skew	0	5.4	25	ps
Tr/Tf Output Rise/Fall Times (20%-80%) @ 1GHz	40	60	80	ps

Characteristics assume all outputs loaded with 50 Ω to (CLK Output Level – 1.5V).

*When using the 1.65V output level and terminating to Ground, the minimum output voltage amplitude is 220mV.

**The levels are based on a 50 Ω termination resistor from the outputs to Vtt-out. For minimum power and maximum product lifetime, values of Vtt-out as close as possible to the maximum are recommended.

Table 5-7: Clock Output Jitter

Clock Input Source	÷	Output Frequency (MHz)	Period Jitter (ps)		Cycle-to-Cycle Jitter (ps)	
			RMS	Pk-Pk	RMS	Pk-Pk
Oscillator	1	100	1.0	11	1.8	18
Oscillator	2	1244	1.1	11	2.0	19
Oscillator	4	622	1.2	11	2.0	17
Oscillator	8	311	1.5	11	2.4	20
Oscillator	16	155.5	1.6	13	2.7	22
SE Ext.	1	100	1.4	19	2.4	36

Clock Input Source	÷	Output Frequency (MHz)	Period Jitter (ps)		Cycle-to-Cycle Jitter (ps)	
			RMS	Pk-Pk	RMS	Pk-Pk
SE Ext	1	500	0.97	11	1.7	19
SE Ext	1	1000	1.0	11	1.7	20
SE Ext	1	1244	0.95	9.6	1.6	17
SE Ext	2	100	1.0	9.8	1.8	17
SE Ext	2	500	.99	12	1.7	20
SE Ext	2	1000	1.2	13	2.1	23
SE Ext	2	1244	1.0	10	1.7	16

Jitter measurements from the Single-Ended External input (SE Ext) were performed with a 15dBm sine wave input produced by an Agilent® 8664A Signal Generator. Actual results when using the external clock input are dependent on the jitter of the input source. All measurements performed with 1.65V PECL outputs and based on 100,000 acquisitions at ambient temperature. Better RMS jitter results in the range of 600-800 fs have been obtained using a sampling scope.

Table 5-8: Clock Output Positive Duty Cycle

Clock Input Source	÷	Output Frequency (MHz)	Positive Duty Cycle (%)		
			Minimum	Typical	Maximum
Oscillator	1	100	48.0	48.6	49.0
Oscillator	1	2488	43.3	49.4	54.0
Oscillator	2	1244	49.3	50.0	50.7
Oscillator	4	622	49.3	50.0	50.4
Oscillator	8	311	49.7	50.0	50.2
Oscillator	16	155.5	49.8	50.0	50.1
SE Ext.	1	100	48.2	48.4	48.6
SE Ext	1	500	48.5	49.1	50.0
SE Ext	1	1000	49.0	50.1	51.8
SE Ext	1	1500	45.9	47.4	49.3
SE Ext.	2	100	49.9	50.0	50.1
SE Ext	2	500	49.2	49.8	50.3
SE Ext	2	1000	49.4	50.1	50.9
SE Ext	2	1500	48.9	49.9	51.3

Duty cycle measurements from the Single-Ended External input (SE Ext) were performed with a 15dBm sine wave input produced by an Agilent® 8664A Signal Generator. Actual results when using an external input and no clock division are dependent on the duty cycle of the input source. All measurements performed with 1.65V PECL outputs and based on 100,000 acquisitions at ambient temperature.

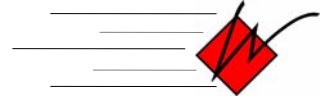
Table 5-9: Trigger Outputs

Characteristic	Minimum	Typical	Maximum	Units
Voh Output High Voltage				
TRIG Output Level 3.3V	2270	2330	2380	mV
TRIG Output Level 2.5V	1500	1560	1610	
TRIG Output Level 1.65V	640	700	750	
Voutpp Output Voltage Amplitude	300	370	400	mV
Vtt-out Termination Voltage*				
TRIG Output Level 3.3V	1295	1485	1800	mV
TRIG Output Level 2.5V	495	740	1010	
TRIG Output Level 1.65V	-355	0	150	
Iout Output Current				
Continuous			25	mA
Surge			50	
Trigger Output to Output Skew	0	6.5	25	ps
Clock to corresponding Trigger Output Delay**	75	100	125	ps
Tr/Tf Output Rise/Fall Times (20%-80%) @ 1GHz	40	60	80	ps

Characteristics assume all outputs loaded with 50 ohms to (TRIG Output Level – 1.5V).

* The levels are based on a 50 Ω termination resistor from the outputs to Vtt-out. For minimum power and maximum product lifetime, choose values of Vtt-out as close as possible to the maximum. The Vtt-out levels specified as typical are the levels used to terminate the unused inverted output, TRIG-. (See Figure 4-6).

** Trigger Output measured with 1.65V PECL outputs and based on an assumed 550mV transition threshold.



6 TECHNICAL SUPPORT

If you have any questions about installing, operating, or maintaining the WILDSTAR™ Clock Synchronization Distribution board, please call the WILDSTAR™ Customer Support staff at (410) 841-2514, fax at (410) 841-2518, or send e-mail to wftch@annapmicro.com.