

WILDSTAR™ PRO 1.5 GHz Analog-to-Digital Converter I/O Daughter Card

Reference Manual

13408–0000 Revision 1.6

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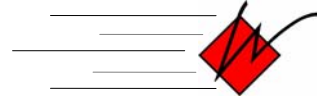
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1. ABOUT THIS MANUAL

This manual provides guidance for installing and using the PRO 1.5 GHz Analog-to-Digital Converter I/O Daughter card, among the newest of the WILDSTAR™-II series I/O cards produced by Annapolis Micro Systems, Inc. This card is compatible with WILDSTAR™-II PRO-series PCI and VME boards, including the single-PE PRO ACE for VME board.



CAUTION

The PRO 1.5 GHz A/D I/O card can also be used with WILDSTAR™-II non-PRO boards, but *only* if the WILDSTAR™-II board is equipped with a factory-configured, Type III I/O card option. Serious damage can occur if a motherboard without this option is used with the I/O card.

The PRO 1.5 GHz A/D I/O card is fully compatible with the CoreFire™ Design Suite, an FPGA design application developed by Annapolis Micro Systems, Inc. As a dataflow-based FPGA design tool, CoreFire™ allows you to create designs in a fraction of the time required for a conventional VHDL-based control flow approach. CoreFire™ can be used to program PEs on WILDSTAR™-II motherboards of all types.

For VHDL users, full support is provided with the PRO 1.5 GHz A/D I/O card.



INFORMATION NOTE

When boards are referred to in this document, the following abbreviations are used:

- **“PRO GHz A/D I/O card”** stands for the PRO 1.5 GHz Analog-to-Digital Converter I/O Daughter card, unless specifically indicated otherwise.
- **“WILDSTAR™-II”** stands for WILDSTAR™-II /VME and /PCI boards, unless specifically indicated otherwise.
- **“WILDSTAR™-II PRO”** stands for WILDSTAR™-II PRO /PCI, PRO/VME, and PRO ACE for VME boards, unless specifically indicated otherwise.

1.1 Chapter Overview

- Chapter 1, “**About This Manual**,” outlines the conventions, icons, and key words used throughout the manual.
- Chapter 2, “**Introduction to the WILDSTAR™ PRO 1.5 GHz A/D I/O Card**,” discusses its architecture and performance features.
- Chapter 3, “**Getting Started**,” describes how to properly unpack and inspect the card.
- Chapter 4, “**Installing the WILDSTAR™ PRO 1.5 GHz A/D I/O Card**,” explains how to install the card and the software included with it. Installation instructions are provided for all motherboard options.
- Chapter 5, “**Technical Support**,” provides information for contacting the Annapolis Micro Systems, Inc. Technical Support team.
- Chapter 6, “**Hardware Reference**,” includes electrical and power specifications, clock input and sourcing options for the card.
- Chapter 7, “**VHDL Support**,” describes in detail the VHDL provided with the card.
- Chapter 8, “**VHDL Design Cycle**,” describes the WILDSTAR™-II VHDL design cycle.




1.2 Conventions

A variety of text styles are used throughout this manual to call attention to specific items:

Convention	Description
Text represented as Screen display	This typeface is used to represent displays appearing on the screen, such as: at the “A:\” prompt.
Text represented as commands	This typeface is used to represent commands that are to be entered, such as: type “setup.”
Text represented as <i>Signal Name</i>	This typeface is used to represent signal names, such as <i>MODE</i> , <i>DIV01</i> .

1.3 Icons

Throughout the manual, important information is highlighted with icons:

Icon	Description
	Information Notes call attention to important features or instructions.
	Cautions are directions that must be followed in order to avoid loss of system data and/or damage to hardware.
	Warnings are directions that must be followed to ensure personal safety.

1.4 Key Words and Definitions

Some of the terms used throughout the manual are defined below.

ADC

Analog-to-Digital converter. The device on the PRO GHz A/D I/O card that digitizes analog signals.

API

Application Programming Interface. A set of functions coded in the C language allowing communication between an application and the WILDSTAR™ board.

CoreFire™ Design Suite

An FPGA design application created by Annapolis Micro Systems, Inc. It contains modular cores used to construct dataflow-based designs for PEs on WILDSTAR™-II motherboards and I/O cards.

ENOB

Effective Number of Bits

External I/O

External Input/Output (I/O)

LVC MOS2

Low Voltage CMOS (2.5 Volts).

LV TTL

Low Voltage TTL (3.3 Volts).

Motherboard

WILDSTAR™-II motherboard hosting the PRO 1.5 GHz A/D I/O card.

MICTOR®™

Matched Impedance Connector System. MICTOR® is a trademark of AMP, Inc.

_n

Signal name suffix denoting active low signal levels.

PE

Processing Element. A Xilinx® Virtex™ Field Programmable Gate Array (FPGA), comprising the main processing element on the PRO 1.5 GHz A/D I/O card.

SFDR

Spur-Free Dynamic Range

SNR

Signal-to-Noise Ratio

SSTL-2

2.5 Supply Voltage-based interface standard for digital integrated circuits per EIA-JEDEC Standard No 8-9.

SSTL-3

A 3.3V Supply Voltage-based interface standard for digital integrated circuits per EIA-JEDEC Standard No 8-8.

VCO

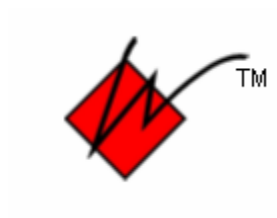
Voltage-Controlled Oscillator

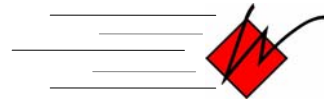
WILDSTAR™, WILDSTAR™-II Host Software

Software provided for the specific WILDSTAR™-II or WILDSTAR™-II PRO motherboard being used. Application examples, device drivers, VHDL models, and APIs are instances of such software.

WILDSTAR™-II, WILDSTAR™-II PRO VHDL Models

Hardware models used for board-level VHDL simulation of applications.





2. WILDSTAR™ PRO 1.5 GHz A/D I/O CARD

2.1 Overview

The WILDSTAR™ PRO GHz A/D I/O card combines rapid analog-to-digital signal conversion with additional processing and memory bandwidth. With these capabilities, the card can provide signal conditioning before data is passed to the motherboard. Sample rates can be as high as 1.5 GHz, depending on the Analog-to-Digital Converter (ADC) model installed on the card (see features list below).

The PRO 1.5 GHz A/D I/O card also supplies a Xilinx® XC2VP70 FPGA for I/O processing, and up to one gigabyte of synchronous DRAM via four independent memory ports.



CAUTION

The PRO GHz A/D I/O card can be used with WILDSTAR™-II non-PRO boards, but *only* if the WILDSTAR™-II board is equipped with a factory-configured, Type III I/O card option. Serious damage can occur if a motherboard without this option is used with the PRO GHz A/D I/O card.

Either VHDL or CoreFire™ can be used to create FPGA designs for the PRO GHz A/D I/O card. The CoreFire™ Design Suite, a design application tool developed by Annapolis Micro Systems, Inc., makes it possible to create designs in a fraction of the time required for a conventional VHDL-based control flow approach. CoreFire™ can be used to program the I/O card PE mounted on a compatible Annapolis Micro Systems motherboard.

2.2 Features

- 1 or 1.5 GHz Max Input Sample Rate
- One Virtex™-II Pro FPGA Processing Element –XC2VP70-5, -6, or -7
- 8-Bit A/D conversion with MAXIM® MAX 104 or 108 Analog-to-Digital Converter. Detailed specifications for both MAX converter models are available at www.maxim-ic.com

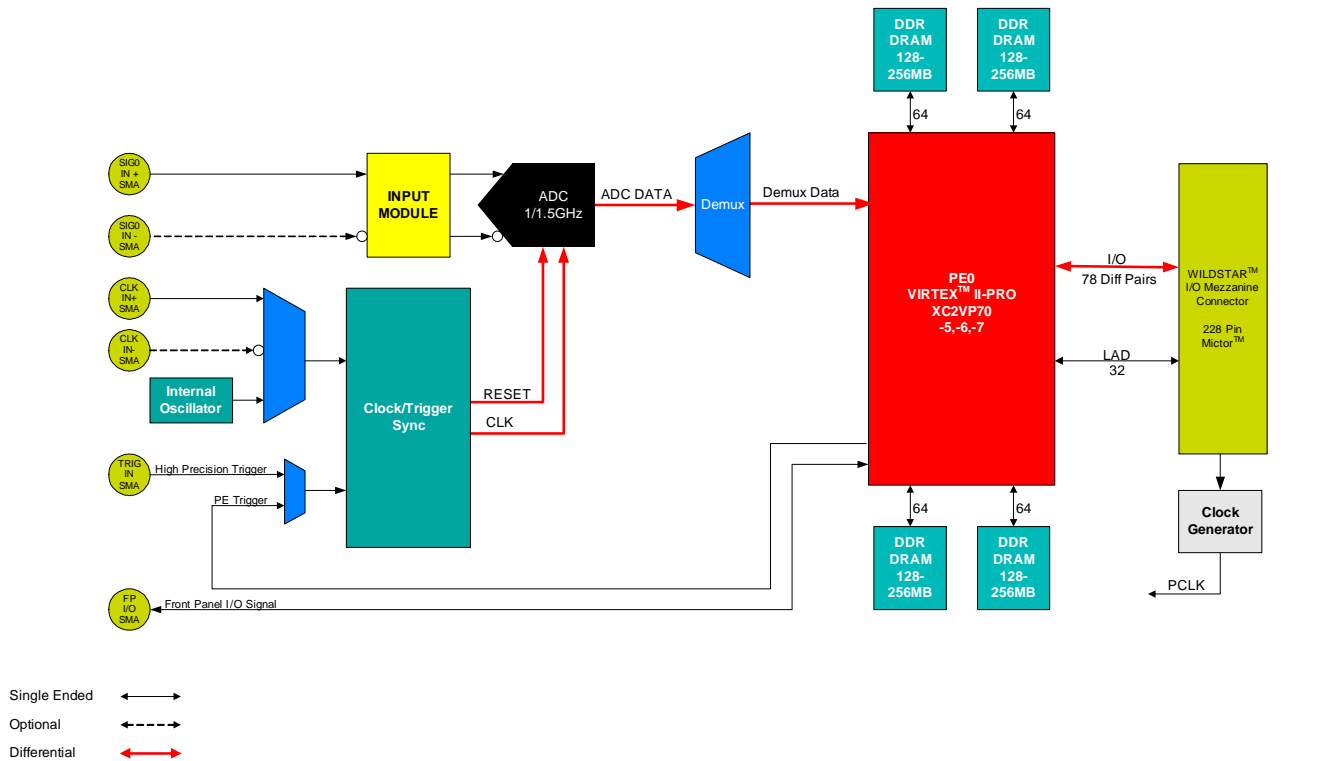
- Four analog input configuration options:
 - Balun
 - Transformer
 - Transistor
 - Differential
- Three High-Precision Trigger Input options: 1.65V LVPECL, 2.5V LVPECL, 3.3V LVPECL
- Internal or External Clock options:
 - Internal oscillator
 - Software-selectable control of which clock is used (Internal/External)
- External clock can be driven from an AC-coupled signal generator or 1.65V LVPECL clock source, or optionally from an LVDS clock source.
- General Purpose Front Panel I/O Signal, LVTTTL, 50 ohms
- 512 MB or 1 Gigabyte of synchronous DRAM
- 4 or more GBytes/Sec I/O bandwidth to motherboard
- Motherboard with I/O card(s) installed occupies a single VME or PCI slot
- Board and FPGA systems speeds up to 200 MHz, depending on motherboard
- Heat sink (VME) or fan with heat sink (PCI) for ADC cooling
- Full CoreFire™ Board Support package, including FFTs, for easy application programming
- Full VHDL support

2.3 PRO GHz A/D I/O Card Architecture

The PRO GHz A/D I/O card architecture is shown in . The card communicates with the motherboard via an external I/O connector on the right side of the block diagram.

The PE on the PRO GHz A/D I/O card is user-configured, which allows much of the digital signal conditioning to be performed on the card before data is forwarded to the motherboard.

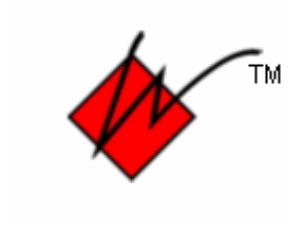
Four analog configuration options are available for the Input Module shown in the diagram below. For additional information about these options, please refer to Chapter 6.

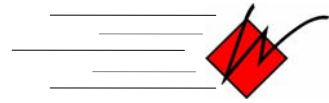


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Figure 2-1: PRO 1.5 GHz A/D I/O Card Block Diagram





3. GETTING STARTED

3.1 Unpacking and Inspecting the Card

The PRO 1.5 GHz A/D I/O card is shipped in a static-sensitive pack. The card should remain sealed in this pack until installation time.



CAUTION

Before removing the card from the static pack, ensure that you are properly grounded against static electricity. Use of a ground strap for this purpose is highly recommended, since static discharge to the PRO GHz A/D I/O card could damage its sensitive components.

Ensure that the following items are included with the card:

DOCUMENTATION

- Reference Manual
- Performance Characterization
- Performance Plot

CD-ROMs

- VHDL, Models and Examples CD-ROM
- PRO GHz A/D I/O card Documentation CD-ROM, containing PDF (portable document file) of this manual

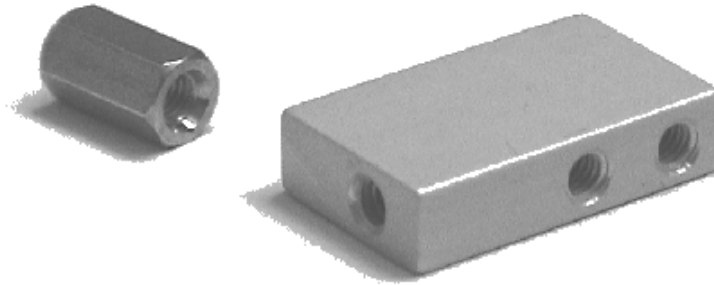
HARDWARE (illustrated below)

For WILDSTAR™- II /VME, PRO/VME, and PRO ACE for VME boards:

- 12 screws
- 6 standoffs

For WILDSTAR™-II /PCI and PRO/PCI boards:

- 14 screws
- 4 standoffs
- Two mounting blocks
- Back plate



Standoff

Mounting Block

(Magnified to show detail)

When handling the card, grasp it carefully by its sides. Avoid touching any of the components on the card's surface, as they are sensitive and can be easily damaged. Visually inspect it for damage that may have occurred during shipping. If you notice any apparent damage to the card or if any items are missing from the shipment, contact Annapolis Micro Systems, Inc. using the information provided in Chapter 5 of this manual.

3.2 Card Components



CAUTION

To reduce heat buildup, the PRO GHz A/D I/O card is equipped with a heat sink. The A/D converter junction temperature on the card should *never* exceed 140 C.

Figures in the following pages illustrate major PRO GHz A/D I/O card part locations on component and solder sides. Information on the location and significance of the PRO GHz A/D I/O card LEDs also appears later in this chapter.

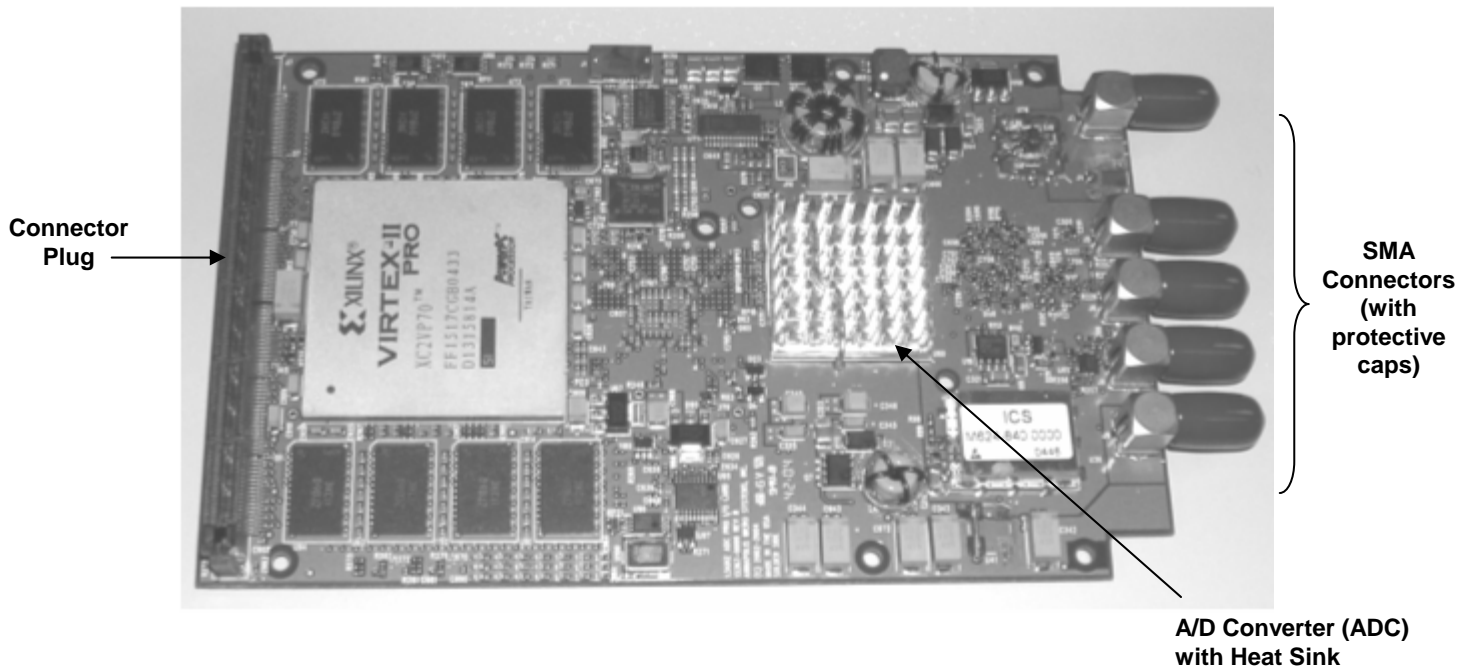


Figure 3-1: PRO GHz A/D I/O Card (Solder Side)

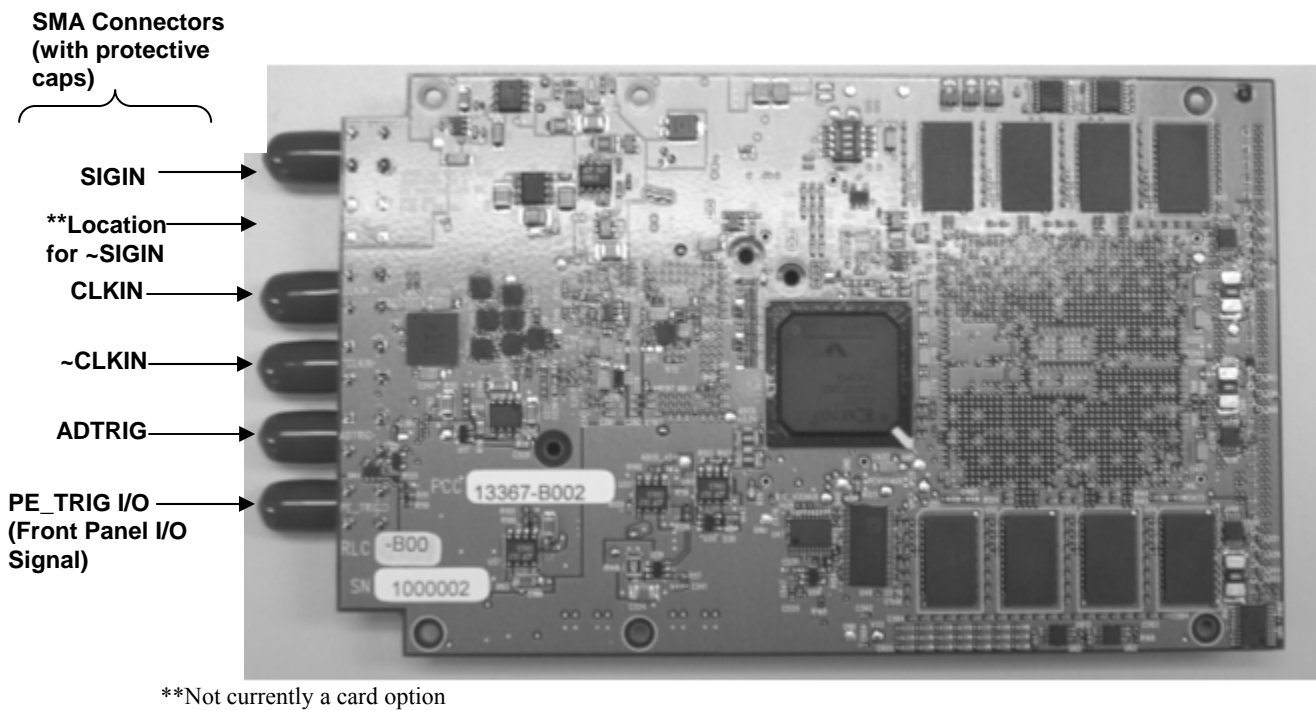
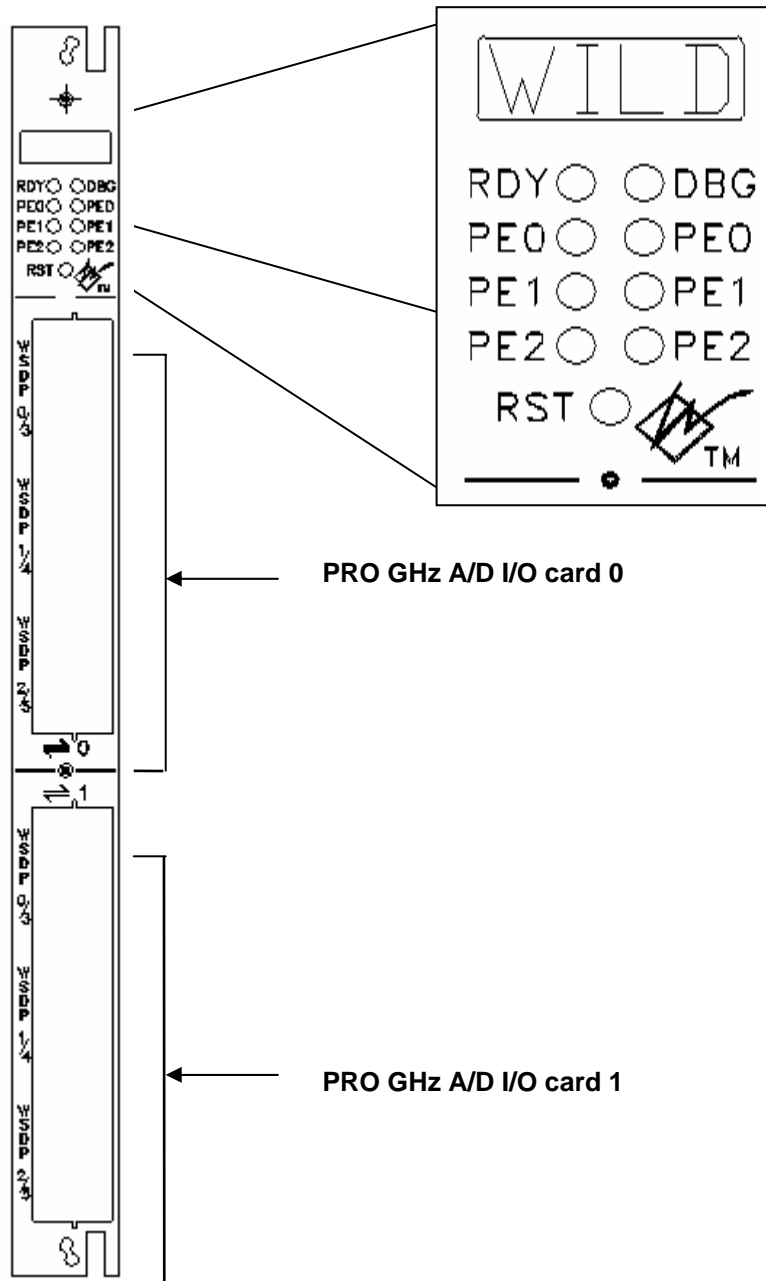


Figure 3-2: PRO GHz A/D I/O Card (Component Side)

3.3 Front Panel—WILDSTAR™-II /VME Motherboard



Note: Disregard WSDP labels on front panel.

Figure 3-3: Front Panel for WILDSTAR™-II/VME

3.4 Back Plate—WILDSTAR™-II PRO/PCI Motherboard

Note that connector designations are stamped on the back plate. For locations of each of these designations, see Figure 3-2.



Figure 3-4: PRO GHz A/D I/O Card Back Plate for use with a WILDSTAR™-II PRO/PCI Board

3.5 LED Displays on the PRO GHz A/D I/O Card

LED functional and diagnostic displays reside on the component side of the PRO GHz A/D I/O card (see figures and table below). If the card is used with an open chassis, the LEDs can provide useful diagnostic and performance information during application development.

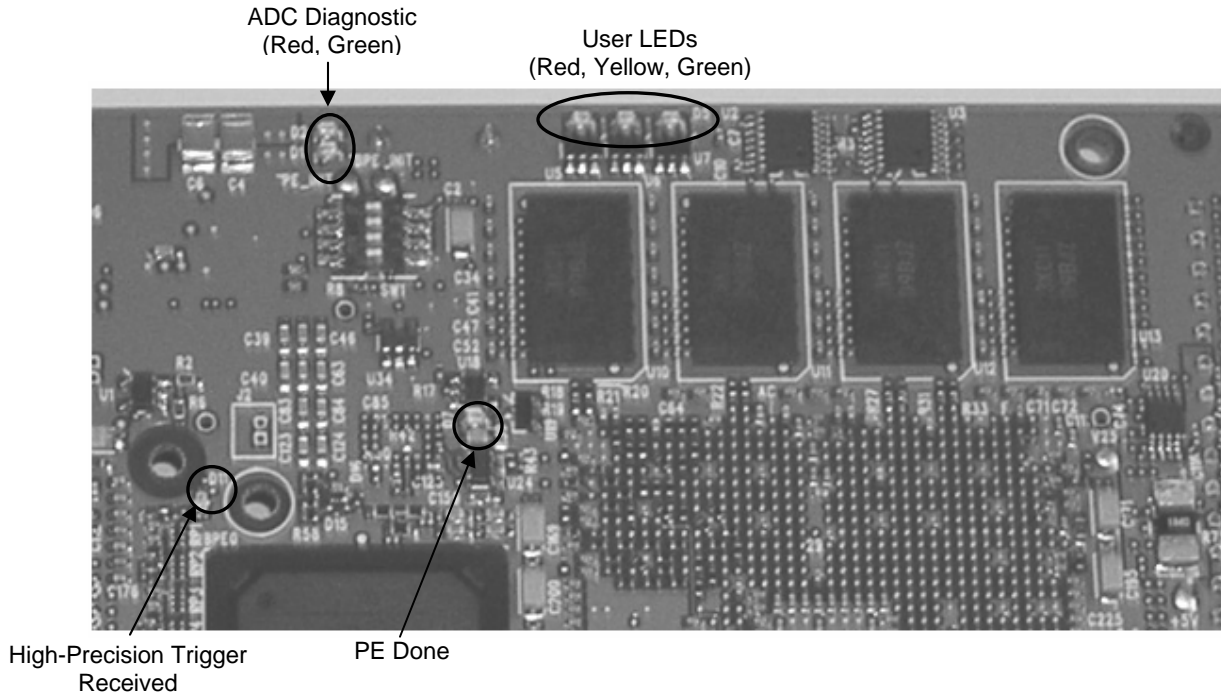


Figure 3-5: LEDs (Component Side, Detail 1)

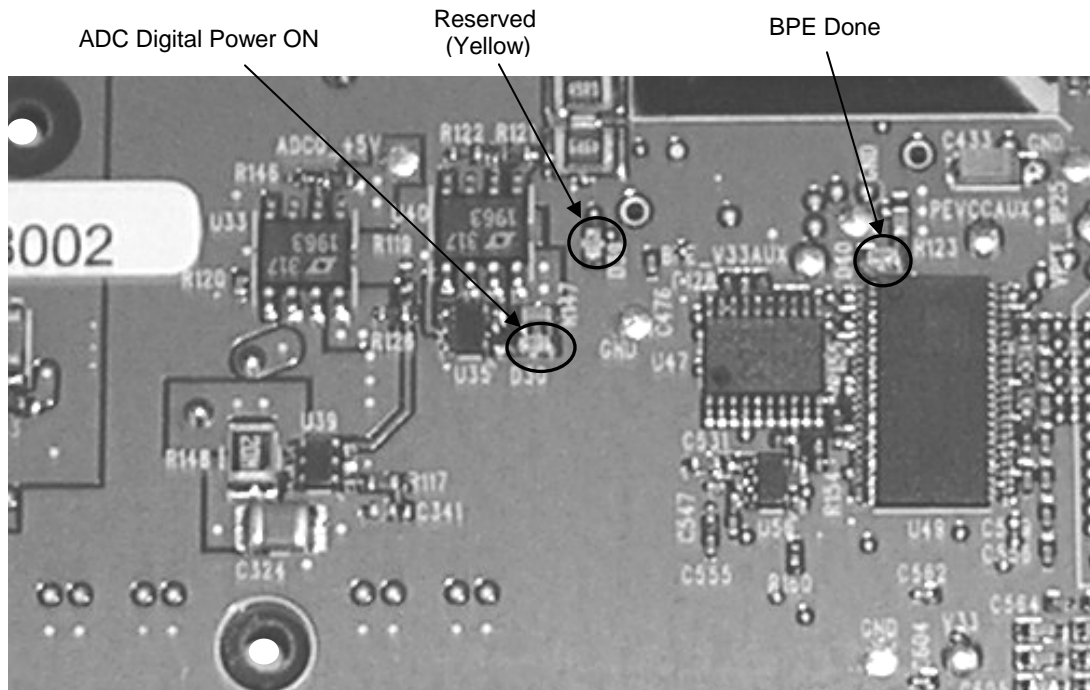
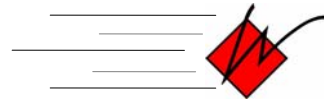


Figure 3-6: LEDs (Component Side, Detail 2)

LED Name	Board Label	LED Color	LED Definition
ADC Diagnostic (2)	D1	Green	--Green ON: Ready to send ADC data to PE --Green OFF: Waiting for Bridge PE initialization to complete.
	D2	Red	--Red ON: Negative voltage for the ADC is not at proper level. --Red BLINKING: Negative voltage for ADC is at proper level, but --Bridge PE has not locked to sample clock. --Red OFF: Negative ADC voltage is at proper level and the Bridge PE has locked to sample clock.
User LEDs (3)	D5	Red, Yellow, Green	User-Defined
PE Done	D7	Green	ON: PE Programmed
High-Precision Trig Received	D11	Yellow	BLINKS one or more times: High-Precision Trigger Received
ADC Digital Power On	D30	Green	ON: ADC Digital Power is on
Reserved	D39	Yellow	Reserved
BPE Done	D40	Green	ON: Bridge PE programmed





4. INSTALLING THE PRO 1.5 GHz A/D I/O CARD

4.1 System Requirements

In order to take advantage of all features of the PRO GHz A/D I/O card, the computer host system should have one or more of the following motherboards:

- WILDSTAR™-II /PCI or /VME PRO motherboard



CAUTION

The PRO GHz A/D I/O card can also be used with WILDSTAR™-II non-PRO boards, but *only* if the WILDSTAR™-II board is equipped with a factory-configured, Type III I/O card option. Serious damage can occur if a motherboard without this option is used with the PRO GHz A/D I/O card.

For specific system requirements, see the *WILDSTAR™ -II Hardware Reference Manual* shipped with the motherboard.

4.2 PRO GHz A/D I/O Card Compatibility

The PRO GHz A/D I/O card is fully compatible with the WILDSTAR™-II /VME and WILDSTAR™-II /PCI PRO-series motherboards. (See Caution note in Section 4.1 regarding use with WILDSTAR™-II non-PRO-series motherboards.)



CAUTION

The A/D converter (ADC) junction temperature on the card should *never* exceed 140 C. Card PE and BPE core temperatures should be kept below 85°C to guarantee accurate timing function.

INFORMATION NOTE

i

If you are mounting the PRO GHz A/D I/O card on a WILDSTAR™-II /PCI 2nd I/O Card Adapter, fan number two must first be removed from the card adapter in order for the I/O card to fit on the adapter. This fan is the one farthest from the adapter ribbon cable.

4.3 Hardware Installation

This section provides diagrams and a series of steps for installing the PRO GHz A/D I/O card. Two sets of installation instructions are included here—one for WILDSTAR™-II/VME and WILDSTAR™-II PRO/VME (including PRO ACE for VME), and one for WILDSTAR™-II /PCI and PRO/PCI.

INFORMATION NOTE

To ensure proper contacts at the SMA connectors, make sure the connector plug screws in easily, indicating proper alignment, and tighten until secure. When using a wrench, a torque of 60-100 Ncm is recommended.

4.3.1 Installing Card on a WILDSTAR™-II /VME, PRO/VME, or PRO ACE

To install the card on a WILDSTAR™-II /VME or PRO ACE for VME motherboard, follow the steps listed below.

INFORMATION NOTE

i

Follow Steps 1-5 if the motherboard is installed in the host computer. Once the board has been removed from the computer, follow Steps 6-15.

CAUTION

!

The PRO GHz A/D I/O card can be used with WILDSTAR™-II non-PRO boards, but *only* if the WILDSTAR™-II board is equipped with a factory-configured, Type III I/O card option. Serious damage can occur if a motherboard without this option is used with the PRO GHz A/D I/O card.

1. Connect the anti-static ground strap.
2. Shut down the host system and power off.
3. If necessary, remove the cover to the VME chassis in order to gain access to the motherboard.
4. Use the VME board ejectors to release the board from the slot.
5. Remove the board from the chassis.

6. With the Allen wrench provided, remove the top, bottom, and middle screws securing the front panel to the motherboard. Next, remove two additional screws adjacent to the front panel ejectors (these are accessible on the solder side of the board). Once these screws are removed, *gently* pull the front panel away from the board. Be especially careful not to tug at the thin ribbon connecting the LED face to the board.
7. Place the motherboard component-side up on a flat electrostatic-protected surface.
8. The PRO GHz A/D I/O card is attached directly to the motherboard with standoffs and hex screws included with the PRO GHz A/D I/O card. The standoffs are anchored with screws through the component side of the PRO GHz A/D I/O card and the solder side of the motherboard.
9. Remove the card from its static-sensitive pack. Hold the card by its edges and place it gently on a flat, electrostatic-protected surface.
10. Attach two standoffs (included with the card package) to the solder side of the card, using two of the hex screws provided to secure the standoffs.
11. Align the connector plug on the solder side of the PRO GHz A/D I/O card with the connector receptacle on the motherboard.
12. Install the PRO GHz A/D I/O card by pressing gently above the connectors until the connectors are firmly seated.
13. Secure the card with four of the hex screws provided (see Figure 4-2).
14. Slide the front panel over the card's SMA connectors. Replace the screws removed in Step 6.
15. Reinstall the motherboard with the mounted PRO GHz A/D I/O card into the computer. Refer to the installation section of the *WILDSTAR™-II Reference Manual*, if necessary.

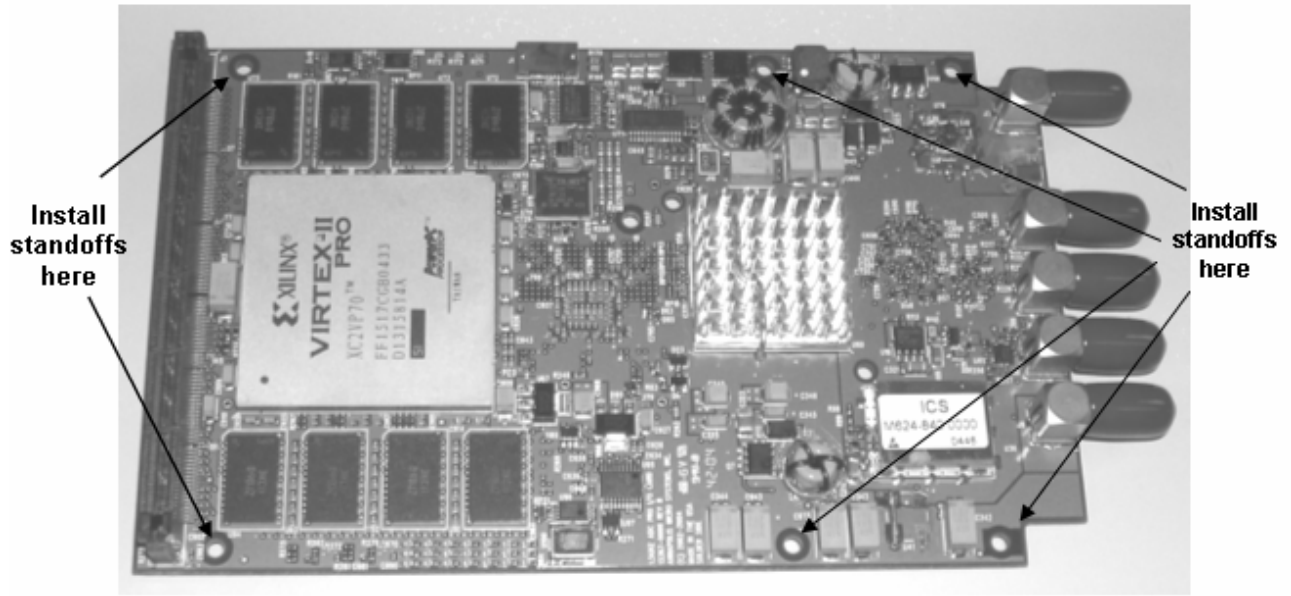


Figure 4-1: PRO GHz A/D I/O Card (Solder Side) Standoff Locations

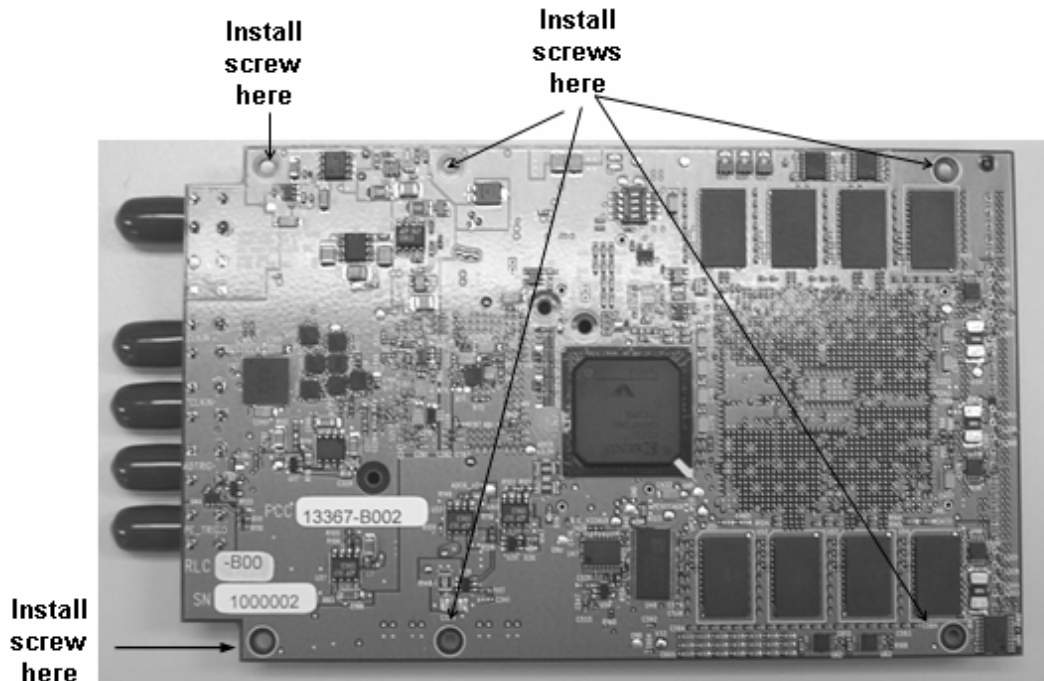


Figure 4-2: PRO GHz A/D I/O Card (Component Side) Screw Locations

4.3.2 Removing Card from a WILDSTAR™-II, PRO /VME, or PRO ACE

To remove the PRO GHz A/D I/O card from the VME motherboard, follow the steps listed below.

1. Connect the ground strap to yourself.
2. Shut down the host system and power off.
3. If necessary, remove the cover to the system chassis in order to gain access to the motherboard.
4. Remove any installed cables.
5. Use the VME ejector handles to release the board from the slot.
6. Remove the motherboard from the chassis.
7. Remove the top, bottom, and middle screws securing the front panel to the motherboard. Next, remove two additional screws adjacent to the front panel ejectors (these are accessible on the solder side of the board). Once these screws are removed, *gently* pull the front panel away from the board. *Be especially careful of the thin ribbon connecting the LED face to the motherboard.*
8. Place the motherboard component-side up on a flat electrostatic-protected surface.

9. Remove the six screws attaching the PRO GHz A/D I/O card to the motherboard. Two of the screws (the ones holding the standoffs) will be accessible on the solder side of the motherboard. The PRO GHz A/D I/O card is attached directly to the motherboard with six standoffs and screws.
10. Using a gentle rocking motion, unseat the I/O card connector plug from the motherboard connector receptacle. Remove the card.
11. Remove the two standoffs described in Section 4.3.1, Step 10.
12. Carefully store the card in a static-sensitive pack. Reserve the spacers, standoffs, and screws for future use.
13. Replace the motherboard front panel and secure with screws.

To reinstall the motherboard, refer to the installation section of the *WILDSTAR™-II Hardware Reference Manual*.

4.3.3 Installing Card on a WILDSTAR™-II /PCI or PRO/PCI

To install the card on a WILDSTAR™-II /PCI motherboard, follow the steps listed below.



INFORMATION NOTE

Follow Steps 1-5 if the motherboard is installed in the host computer. Once the board has been removed from the computer, follow Steps 6-15.

1. Connect the anti-static ground strap.
2. Shut down the host system and power off.
3. If necessary, remove the cover to the chassis to gain access to the motherboard.
4. Remove the upward-facing screw securing the steel back plate of the motherboard to the chassis, then lift out the board and the attached back plate.
5. Remove the two screws holding the standard back plate to the motherboard. Lay the back plate aside.
6. Place the motherboard component-side up on a flat electrostatic-protected surface.
7. Remove the card from its static sensitive pack. Hold the card by its edges and place it carefully on a flat electrostatic protected surface.

8. Attach four standoffs (included with the card) to the component side of the motherboard by securing them with four 4mm hex screws. Screw them in from the solder side.
9. Attach two mounting blocks to the component side of the motherboard by securing them with two hex screws through the motherboard's solder side. The off-center screw hole in the side of each mounting block should be closest to the motherboard.
10. Align the connector plug on the solder side of the PRO GHz A/D I/O card with the connector receptacle on the motherboard.
11. Press the card gently against the connector receptacle until the connector is completely seated.
12. Install six hex screws (packaged with the PRO GHz A/D I/O card assembly) through the component side of the I/O card. Four of these screws will go into the standoffs, while two will go into the tops of the mounting block screw holes.
13. Locate the back plate provided with the I/O card and slide it over the cable receptacle. Attach it to the mounting blocks using two of the screws provided.

Reinstall the motherboard with the mounted PRO GHz A/D I/O card into the computer. Refer to the installation section of the *WILDSTAR™-II Reference Manual*, if necessary.

4.3.4 Removing Card from a WILDSTAR™-II /PCI or PRO /PCI

To remove the card from a PCI motherboard, follow the directions listed below.

1. Connect the ground strap to yourself and power off the host computer.
2. If necessary, remove the cover to the system chassis in order to gain access to the motherboard.
3. Carefully remove any installed cables.
4. Remove the upward-facing screw securing the steel back plate of the PCI motherboard to the chassis, then lift out the board and the attached back plate.
5. Remove the two screws holding the back plate to the mounting blocks on the motherboard. Lay the back plate aside.
6. Place the motherboard component-side up on a flat electrostatic protected surface.
7. Remove the six screws attaching the card to the motherboard.
8. Using a gentle rocking motion, unseat the I/O card connector plug from the motherboard connector receptacle. Remove the card.

9. Remove the four standoffs from the motherboard.
10. Also, remove the two mounting blocks from the motherboard.
11. After removal, store the card in a static-sensitive pack. Reserve the installation hardware for future use.
12. Replace the standard back plate to the motherboard and secure with two screws.

To reinstall the PCI motherboard, refer to the installation section of the *WILDSTAR™-II Hardware Reference Manual*.

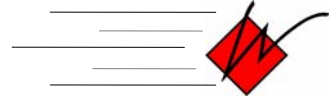
4.4 Cable Requirements and Installation

The PRO GHz A/D I/O card requires 50 ohm SMA connectors and cables (sold separately) for inputs and outputs. External clock connections also require SMA connectors and cables.

4.5 Switch Settings

Table 4-1: PRO 1.5GHz A/D I/O Card Switch Settings

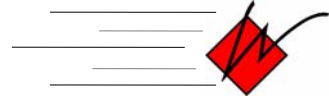
Switch 1 Position	Name	Default Position
1	Reserved	Leave in OFF Position
2	Reserved	Leave in OFF Position
3	Reserved	Leave in OFF Position
4	Reserved	Leave in OFF Position



5. TECHNICAL SUPPORT

If you have any questions about installing, programming, using, or maintaining your PRO 1.5 GHz A/D I/O card, please call the WILDSTAR™ Customer Support staff at (410) 841-2514, fax at (410) 841-2518, or send e-mail to wftch@annapmicro.com.





6. HARDWARE REFERENCE

6.1 PRO 1.5 GHz A/D I/O Card Hardware

This chapter contains hardware reference information for the PRO GHz A/D I/O card, including electrical specifications, clocking, and input options.

6.2 General Specifications

Table 6-1 specifies the physical dimensions and operating range for the card:

Table 6-1: PRO 1.5 GHz A/D I/O Card Specifications

Physical Dimensions:	Length: 149.7mm/5.89 in Width: 91.44mm/3.6 in Thickness: 1.325mm/.053 in
Operating Range:	Temperature: 0° to 85°C

6.2.1 Heat Specifications and Advisory

It is critical that heat limits for the PRO GHz A/D I/O card be observed. For cards in a VME chassis, airflow of at least 400 LFM per slot should be maintained and the A/D converter junction temperature kept below 140°C. Card PE and BPE core temperatures should be kept below 85°C to guarantee accurate timing function.

WARNING

When mounted on a WILDSTAR™-II PRO /VME or PRO ACE motherboard, the PRO GHz 1.5 A/D I/O card is equipped with a heat sink on the MAXIM ADC part. When mounted on a WILDSTAR™-II /PCI or PRO/PCI motherboard, the I/O card is cooled by both a heat sink and cooling fan.

To prevent system damage, fire, and personal injury, never use any of these boards without the proper heat reduction components installed and functioning.

6.3 Power Consumption Limits

Below are some important cautionary statements for power consumption.



CAUTION

According to VME specifications, the total power should not exceed **35** watts per slot. According to VME64X specifications, the total power per slot should not exceed **45** watts. Ensure that the base system is capable of supplying adequate power and cooling to run the application.



CAUTION

According to PCI specifications, the total power should not exceed **25** watts per slot. If the estimated power consumption for an application exceeds 25 watts per slot, ensure that the base system is capable of supplying adequate power and cooling to run the application.

6.4 Available Input Signal Options for the PRO GHz I/O Card

Four factory-configured input signal module options are available for the PRO GHz A/D I/O card:

- Balun
- Transformer
- Transistor
- Differential

Inputs through all options are terminated through 50 ohms to Ground.

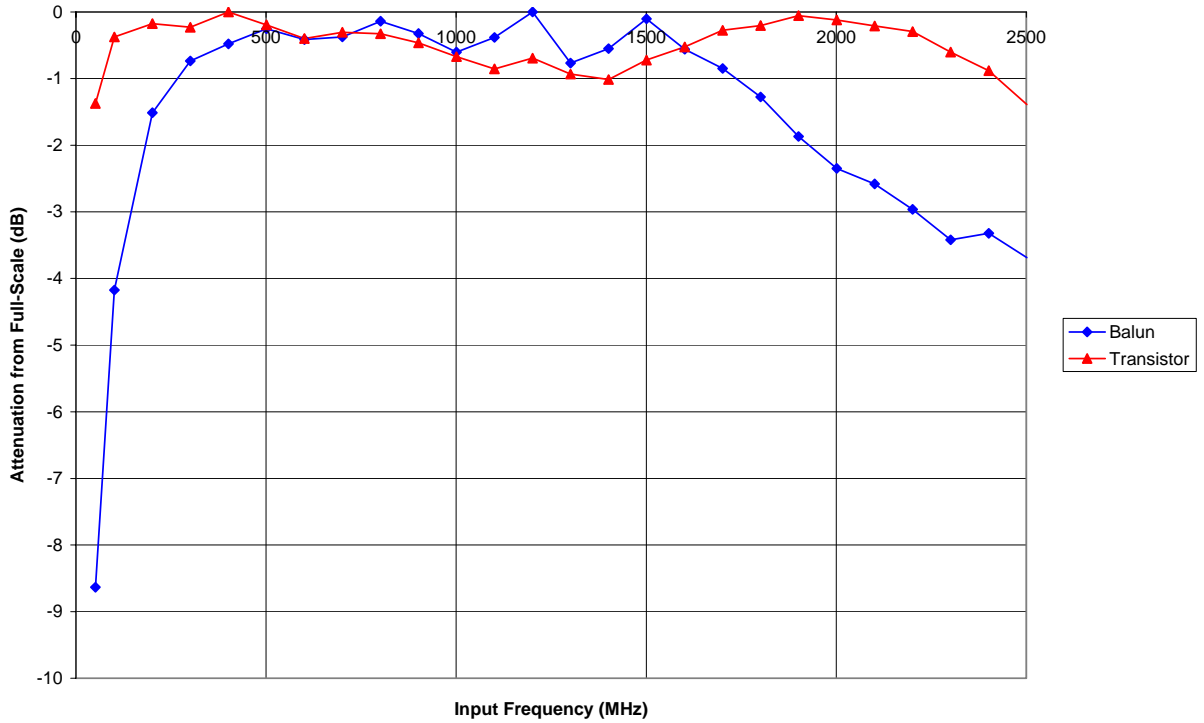
The tables below show bandwidth and power for the Dual GHz A/D I/O card. These numbers are approximate to the performance expected for the PRO GHz A/D I/O card.

Table 6-2: Input Bandwidth

Input Module	Frequency Bandwidth (3dB)
Balun	140-2200 MHz
Transformer	5-950 MHz
Transistor	50-2500 MHz
Differential	TBD

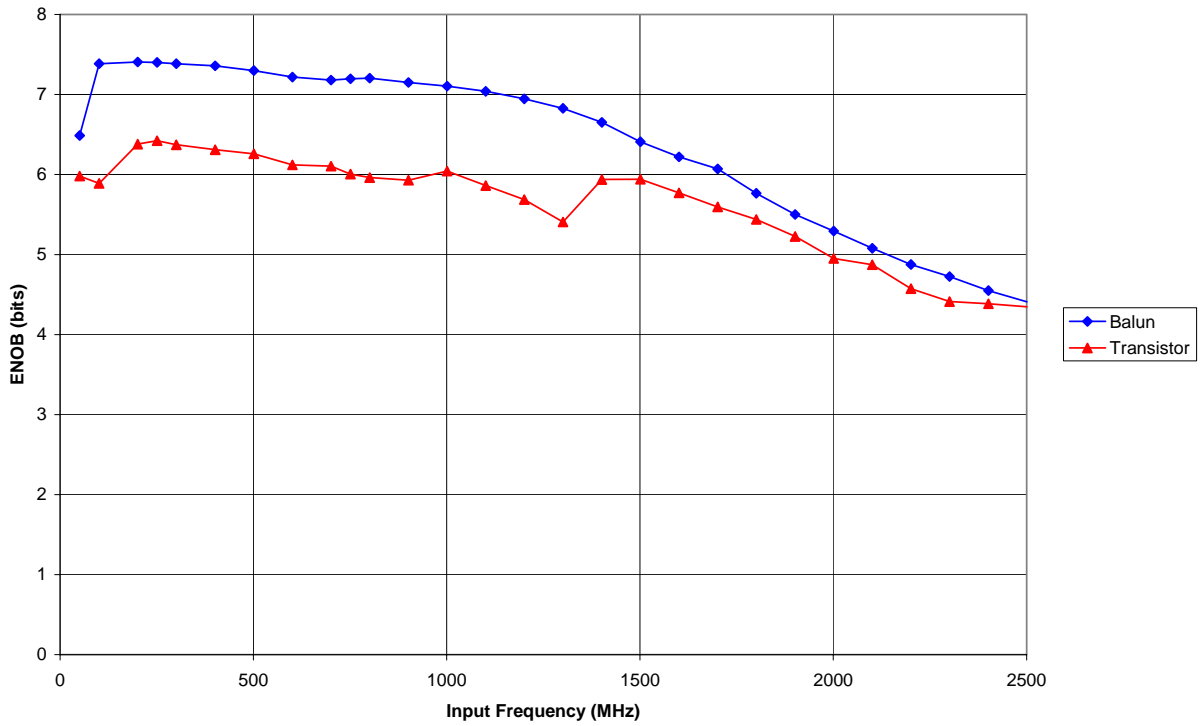
Table 6-3: Full-Scale Input Power

Input Module	Input Frequency	Full-Scale Input Power (50 Ohms)
Balun	800 MHz	-2.0 dBm +/- 0.5 dBm
Transformer	50 MHz	-1.7 dBm +/- 0.5 dBm
Transistor	800 MHz	-0.6dBm +/- 0.5 dBm



*Transformer and Differential input performance are TBD

Figure 6-1: Average Frequency Response, All Available Input Options



*Transformer and Differential input performance are TBD

Figure 6-2: Average ENOB, All Available Input Options

6.5 PRO GHz A/D I/O Card Clocks

In the PRO GHz A/D clock structure, the motherboard sources MCLK, UCLK, and ICLK. The A/D clock comes from either the onboard oscillator or the SMA input ADEXTCLK.

6.5.1 Clock Sources

The PRO GHz A/D I/O card can be clocked using an external source or an optionally populated internal SAW oscillator.

6.5.1.1 External Clock Input

As specified by the customer, the PRO GHz A/D I/O card is shipped with one of two possible types of A/D converters--MAX 104 or MAX 108. The A/D converter board's sample clock can be supplied externally through the clock SMA connectors. Also, according to customer specifications, the A/D converter board can be configured with an internal SAW oscillator as the sample clock source. The sample internal or external clock source can be selected through software.

Default External Clock Amplitudes

If the "Default" external clock option has been chosen, then the clock can be driven by a sine-wave signal generator with 50 Ohm to GND output; for instance, with an Agilent® 8664A, an Annapolis Micro Systems, Inc. Clock Distribution board, or another LVPECL source having the following output levels:

A/D Clock Frequencies

Minimum: 400 MHz

Maximum: 1500 MHz

Table 6-4: External Clock Amplitudes

V_{OHmax}	2.5V
V_{OLmin}	0V
$V_{threshold}$	0.55V
V_{tt} (expected 50-Ohm termination voltage)	0V

Signal generator clock source amplitude is as follows:

Table 6-5: External Clock Amplitudes

Min = +0dBm
Max = +18dBm
Recommended = +15dBm

For sin-wave signal generators, higher amplitudes have been found to give significantly lower and therefore better clock jitter results. At lower frequencies, the edges of a sin-wave have slower rise times, so raising the amplitude increases the rise time and causes the onboard buffer to sample the clock from edge to edge more accurately.

Jitter approaching 1ps periodic (RMS) or more can significantly affect the noise floor and ENOB of the ADCs, especially at higher signal frequencies. For this reason, a high amplitude of +15dBm is recommended for sin-wave generators.

INFORMATION NOTE

For best signal-to-noise ratio results, use an external clock source with low jitter.

6.6 High-Precision Trigger Input

The single-ended High-Precision Trigger input enters the PRO GHz A/D I/O card via a 50 Ω SMA connector. The input provides a general-purpose control signal that is sampled at the same rate as the analog input signal and passed along in parallel with the signal throughout the digital conversion process.

The High-Precision Trigger is registered and pipelined through delay control logic ensuring that its latency from the TRIG IN connector to the PE has a consistent relationship with the latency of the analog signal from its SIG IN connector to the PE, where it appears as a digital 8-bit sample.

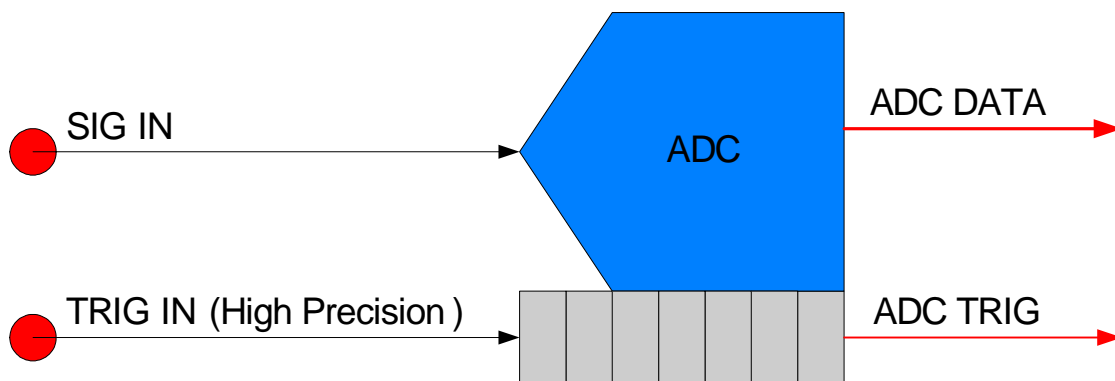


Figure 6-3: Abstract view of the Trigger and Analog Signal Input illustrating their journey from input connectors to a stream of one-to-one pairings of triggers and digital data samples.

The one-to-one relationship between the trigger and data samples presented to the PE makes the trigger ideally suited to mark the start of data collection or to frame a set of sample data. The High-Precision Trigger does not itself start or stop the

flow of data samples. Instead, samples of the trigger can be used within the PE for this purpose.

6.6.1 Synchronizing Multiple Cards

An additional use for the trigger is to synchronize data collection across multiple PRO GHz A/D I/O cards. Synchronizing multiple cards is accomplished by distributing a common clock and a common synchronous trigger signal to each card. If the common trigger is driven from a logic low to a logic high, for example, the data corresponding to the first '1' seen on the trigger in each PE is known to have been sampled on the same clock edge on each card.

When using the High-Precision Trigger Input to synchronize multiple PRO GHz A/D I/O cards, setup and hold timing requirements must be met at the TRIG IN input. These requirements appear in Table 6-6. If the timing requirements cannot be guaranteed, as with an asynchronous trigger input, the relationship between trigger transitions and the data samples may vary by one sample from card to card.

If on-board oscillators, rather than a common external signal, provide the clock to multiple cards, precise synchronization between cards is not possible, as the phase relationship of the clocks cannot be controlled from card to card.

Annapolis Micro Systems, Inc. provides the A/D Clock Synch Distribution board for the purpose of distributing high-speed clocks and triggers to multiple cards. When using the A/D Clock Synch Distribution board as a clock and trigger source, with delay-matched cables for all clock and trigger connections, the trigger input timing requirements of the PRO GHz A/D I/O card are satisfied by design.

INFORMATION NOTE

Note that Rev D of the Clock Distribution board minimum trigger clock-to-output time just meets the minimum required hold time by the PRO GHz A/D I/O card. Therefore, if cables are slightly mismatched, the longer cables should be favored for the trigger inputs.



6.6.2 High-Precision Trigger Input Electrical Characteristics

The High-Precision Trigger Input voltage levels are dependent on a factory-configurable option. Three Trigger Input choices are available for the PRO GHz A/D I/O cards.

- 1.65V LVPECL
- 2.5V LVPECL
- 3.3V LVPECL

The trigger input is terminated through 50 Ω to a voltage level specified as $V_{\text{Termination}}$ in Table 6-6. As such, it is suited for a LVPECL driver, though other drivers are acceptable as long as they are capable of meeting the input requirements specified in Table 6-6. If the driver is series terminated, consider that the 50 Ω parallel termination will reduce the voltage levels seen at the input.



INFORMATION NOTE	
	<p>If the High-Precision Trigger Input is driven by the Annapolis Micro Systems, Inc. A/D Clock Synch Distribution board, the PRO GHz A/D I/O card should be configured with the 1.65V LVPECL trigger input factory option. Likewise, the Distribution board's Trigger Output Level should be set to 1.65V LVPECL.</p> <p>This configuration is necessary because the V_{OLmax} of the Distribution Board's 2.5V LVPECL and 3.3V LVPECL trigger outputs exceed the V_{ILmax} of the corresponding trigger input levels on the Rev B and Rev C PRO GHz A/D I/O cards.</p>

Table 6-6: High-Precision Trigger Input Characteristics

	Minimum	Typical	Maximum	Units
TRIG IN Setup Time with respect to rising edge of CLK IN input*	100			ps
TRIG IN Hold Time with respect to rising edge of CLK IN input*	75			ps
1.65V LVPECL Trigger Option				
V_{IH} Input High Voltage 1.65V LVPECL Option	0.7		2.25	V
$V_{\text{InThreshold}}$ Threshold Voltage 1.65V LVPECL Option		0.55		V
V_{IL}^{**} Input Low Voltage 1.65V LVPECL Option	Greater of -0.8 and ($V_{\text{IHmax}} - 2.8$)		0.4	V
$V_{\text{Termination}}$ Termination Voltage 1.65V LVPECL Option		0		V
2.5V LVPECL Trigger Option				

	Minimum	Typical	Maximum	Units
V_{IH} Input High Voltage 2.5V LVPECL Option	1.45		2.5	V
V_{InThreshold} Threshold Voltage 2.5V LVPECL Option		1.3		V
V_{IL**} Input Low Voltage 2.5V LVPECL Option	Greater of -0.8 and (V _{IHmax} - 2.8)		1.15	V
V_{Termination} Termination Voltage 2.5V LVPECL Option		0.7		V
3.3V LVPECL Trigger Option				
V_{IH} Input High Voltage 3.3V LVPECL Option	2.25		2.5	V
V_{InThreshold} Threshold Voltage 3.3V LVPECL Option		2.1		V
V_{IL**} Input Low Voltage 3.3V LVPECL Option	Greater of -0.8 and (V _{IHmax} - 2.8)		1.95	V
V_{Termination} Termination Voltage 3.3V LVPECL Option		1.48		V

* Timing requirements apply at SMA connector inputs.

** If the trigger input is sourced from a PECL/LVPECL driver, the minimum V_{IL} should exceed V_{Termination} to satisfy PECL output requirements.

6.6.3 Clock and Trigger Input Details

Additional details are presented here for the advanced user who may require a more complete picture of the clock and trigger inputs.

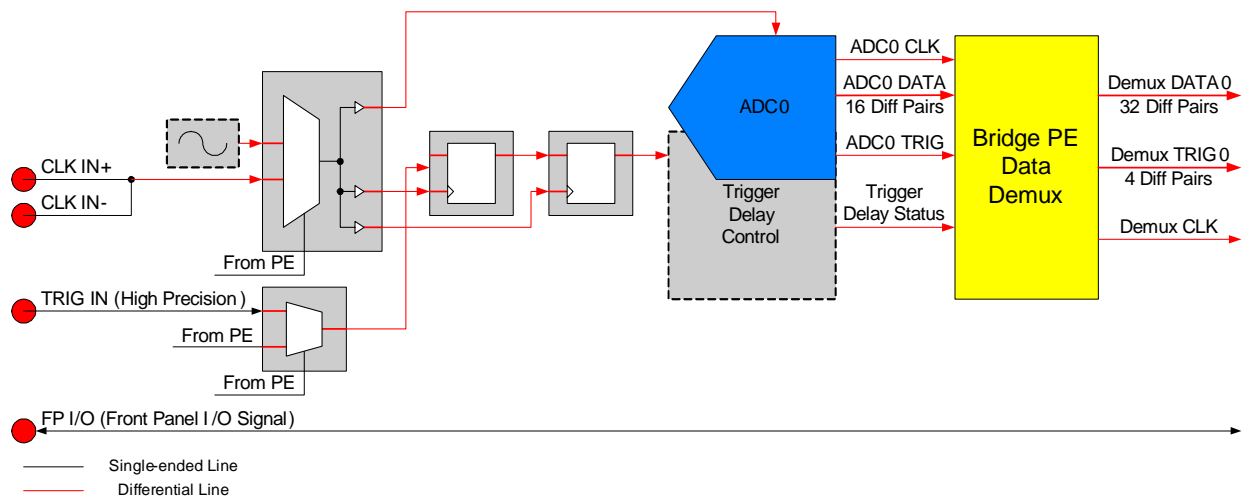


Figure 6-4: PRO GHz A/D I/O Clock and Trigger Inputs

In the detailed illustration of the clock and trigger input paths (Figure 6-4), it is revealed that the High-Precision Trigger Input first passes through a multiplexer, the primary purpose of which is to allow the generation of an on-board “initialization trigger” during ADC reset. The initialization trigger is needed to reset the Trigger Delay Control logic. The ADC reset process that creates this trigger is a part of the `cf_io_reset()` host API call for CoreFire™ users, and is included as a part of example code for the VHDL user.

After the ADC reset, the High-Precision Trigger Input connector is selected as the trigger source for runtime. The presence of the input multiplexer is normally transparent, though it can be exposed in some applications, allowing the PE to generate on-board triggers at runtime for purposes such as debugging.

After the multiplexer, the trigger is clocked by a pair of registers that synchronize the trigger input to the sample clock. To guarantee precise alignment of the triggers on two PRO GHz A/D I/O cards, the trigger setup and hold times must be met at the input connectors (Table 6-6).

Once the signals have been digitized, the data samples are passed along to the Bridge PE along with the trigger samples and other status information used to ensure the proper one-to-one relationship between each trigger and data sample. The Bridge PE demultiplexes the data samples and corresponding triggers to present them to the PE four parallel samples at a time at a fraction of the sample clock rate.

6.7 Front Panel I/O Signal

The Front Panel I/O Signal can be used as either an input or output. It is a simple connection between the SMA connector and the PE, which goes through no intervening logic. It is not intended as a high-speed signal, so timing parameters at the connector are not characterized.

A PE output called ADTRIGTERMSEL determines whether the Front Panel I/O Signal is configured with 50 Ω parallel termination to ground. At power-up and prior to PE programming, ADTRIGTERMSEL is high, enabling the 50 Ω termination.

CAUTION

If the Front Panel I/O Signal is used as an input and if the driver requires 50 Ω termination, make sure the termination is enabled prior to and throughout the period that the signal is applied to the Front Panel I/O connector. Failure to do so could result in voltages outside the limits of Table 6-7, which can damage the card.

When used as an output, the Front Panel I/O Signal has 50 Ω series termination and the optional 50 Ω parallel termination should be disabled by driving ADTRIGTERMSEL low.

In PE designs created with CoreFire™, the ADTRIGTERMSEL signal may be driven automatically, enabling the 50 Ω termination when the Front Panel I/O Signal is configured as an input, and disabling the termination when the Front Panel I/O Signal is configured as an output.

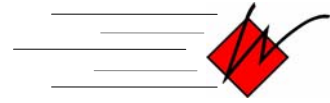
Table 6-7: Front Panel I/O Signal Input Characteristics

	Minimum	Typical	Maximum	Units
V_{IH} Input High Voltage	2.0		3.45	V
V_{IL} Input Low Voltage	-0.2		0.8	V

Table 6-8: Front Panel I/O Signal Output Characteristics

	Minimum	Typical	Maximum	Units
V_{OH} Output High Voltage	2.4			V
V_{OL} Output Low Voltage			0.4	V
I_{OL} Guaranteed Output	24			mA

	Minimum	Typical	Maximum	Units
Current at V_{OL}				
I_{OH} Guaranteed Output Current at V_{OH}	-24			mA



7. PRO 1.5 GHz A/D I/O CARD VHDL SUPPORT

INFORMATION NOTE

i

VHDL specific to the PRO GHz A/D I/O card has been added to the WILDSTAR™-II /PRO mainboard VHDL Model.

VHDL for the PRO 1.5 GHz Analog-to-Digital Converter I/O Daughter card models the whole I/O board and its connection to the mainboard. This includes the I/O card's main PE, the bridge PE, and the A/D converter.

7.1 VHDL Interface Components

As with the mainboard, the PE processing module on the PRO 1.5 GHz Analog-to-Digital Converter I/O Daughter card consists of numerous auxiliary components—clocks, memories, other PEs, and the host interface (LAD) controller—all of which can be used in any design.

Supplied with the VHDL model described are interfaces to each of these components. Each interface component contains the logic necessary to communicate with the component and simplifies the interface presented to the user. The user logic is presented with two records—one containing all input standard interface signals, the other containing all output standard interface signals.

Each interface component includes User_In, User_Out, and Pads ports. The Pads ports connect the component to the pads of the PE. The PE pads are divided into logical sets by record type. For example, a Pads.Clocks record maps to all the clock pads, and a Pads.LAD_Bus record maps to all the LAD bus pads. The Pads port of each interface component are assigned one of these Pads records.

The User_In port is a record of signals that are outputs of the component, but inputs to user logic. Similarly, the User_Out port is a record of signals that are inputs to the component, but outputs of user logic.

In addition to User_In, User_Out, and Pads, each interface component has one or more clock ports. All logic into and out of the interface is synchronous to one of these clocks. Additionally, all Pad output signals are registered in the IOB on their appropriate clock edge.

In addition to User_In, User_Out, and Pads, each core component has a various clock ports. All logic into and out of the interface is synchronous to one of these clock ports.

7.1.1 IO Clock Interface (io_clock_interface)

i

INFORMATION NOTE

It is strongly encouraged that you use only a single clock in a PE design. Use of multiple clocks within a single PE may cause severe clock jitter and application failure. P_clock is recommended for most processing tasks.

IO_Clock_interface provides an interface to the various clock pads and other clock-related information in the VHDL design. The component declaration is shown below:

```
component io_clock_interface is
generic (
  P_CLK_DCM_FREQUENCY_MODE    : string    := "LOW"
);
port (
  pads           : inout io_clock_pads_type;
  reset         : in std_logic;
  reserved      : inout io_reserved_type;
  user_in       : out io_clock_interface_in_type;
  user_out      : in io_clock_interface_out_type
);
end component;
```

The io_clock_interface component has four port signals: pads, reserved, user_in, and user_out. The pads port is the component interface to the PE clock pads. This port should always be assigned to 'pads.io_clocks'. The Reserved port is for "behind-the-scene" signals. This port should always be assigned to 'reserved'.

The user_in port, a record of type io_clock_interface_in_type, is the user interface to the clock inputs. These signals should be used as the clock sources of the design.

Shown below is the definition of the io_clock_interface_in_type record.

```
type io_clock_interface_in_type is record
  p_clock      : io_clock_in_type;
  ref48_clock  : std_logic;
end record;
```

Ref48_clock is a reference clock permanently set at 48 MHz. P_clock is the main processing clock that most of the user code runs on. P_clock uses a Xilinx® DCM, which helps eliminate the effects of clock skew across the FPGA device, but it takes time to acquire a lock to the feedback (or reference) clock. The "locked" indicator flags are provided to the design so you can determine when the DCM has acquired a lock. The host also has access to this information.

The io_clock_in_type record contains all the DCM output signals, shown below:

```

type io_clock_in_type is record
  clock      : std_logic;
  clock90    : std_logic;
  clock180   : std_logic;
  clock270   : std_logic;
  clock2x    : std_logic;
  clock2x180 : std_logic;
  clockdv    : std_logic;
  locked     : std_logic;
  pad        : std_logic;
end record;

```

This record set gives you an interface to most of the DCM outputs for p_clock.

The user_out port, of type io_clock_interface_out_type, provides you with an interface to any of the clock outputs. The record definitions below show the available signals:

```

type io_clock_interface_out_type is record
  p_clock      : io_clock_out_type;
end record;

```

The “reset” signal in clock_out_type gives you the ability to reset the p_clock DCM. This is also available to the host.

```

type clock_out_type is record
  reset      : std_logic;
end record;

```

Details of all the port signals of the clock_interface are shown in Table 7-1.

Table 7-1: IO Clock Interface Component Port Signals

Signal Name	Width	Dir	Description
Pads	NA	Bi-dir	Clock pad signals
Reserved	NA	Bi-dir	Reserved signals
User_In.p_clock	1	Output	Processor clock DCM input record.
User_In.ref48_clock	1	Output	48 MHz reference clock. (Not connected to a DCM)
User_Out.p_clock	1	Input	Processor Clock DCM output record.

The clock interface generics are described below. For most applications they can be left out, since they are all given appropriate default values:

- P_CLK_DCM_FREQUENCY_MODE:** This generic should be set to LOW_FREQ (default) for nearly all applications. The Xilinx® documentation describes this DCM attribute in more detail.

7.1.2 IO LAD Bus Interface (io_lad_interface)

The LAD Bus is the primary means of communicating with the host system. Using the LAD bus, the PE can send and receive programmed I/O data from the host and DMA data to and from the host.

The component declarations for the io_lad_interface and port record types are shown below:

```
component io_lad_interface is
port (
  pads          : inout io_lad_pads_type;
  reset         : in std_logic;
  reserved      : inout io_reserved_type;
  user_in       : out lad_interface_in_type;
  user_out      : in lad_interface_out_type
);
end component;
```

```
type lad_interface_in_type is record
  addr          : std_logic_vector(18 downto 0);
  data_in       : std_logic_vector(31 downto 0);
  reg_strobe    : std_logic;
  dma_strobe    : std_logic;
  dma_in_progress : std_logic;
  write         : std_logic;
  pci_rdy       : std_logic;
  bus_gnt       : std_logic;
  rxclk_in      : clock_in_type;
end record;
```

```
type lad_interface_out_type is record
  data_out      : std_logic_vector (31 downto 0);
  strobe_out    : std_logic;
  dma_init      : std_logic;
  pe_rdy        : std_logic;
  int_req       : std_logic;
  bus_req       : std_logic;
end record;
```

The “user_in” and “user_out” port signals of the io_lad_interface component should be used by the design to receive data from, and send data to, the LAD bus of the WILDSTAR™-II PRO device. The “pads” signals of the io_lad_interface component are only used to connect the lad_interface component to the pads, and should always be assigned to pads.io_lad_bus.

A definition of each of the port signals is given in Table 7-2 below.

Table 7-2: IO LAD Bus Interface Component Port Signals

Signal Name	Width	Dir	Description
-------------	-------	-----	-------------

Signal Name	Width	Dir	Description
pads	NA	Bi-dir	LAD Bus Pad signals
reset	1	Input	Global reset (or set) signal; connected to the GSR input of a STARTUP_Virtex component
Reserved	NA	Bi-dir	Reserved signals
user_in.addr	19	Output	User interface to the LAD bus address; note that this is a DWORD address; also note that this address is automatically incremented each clock cycle during burst LAD bus cycles
user_in.data_in	32	Output	User interface to the input data from the LAD bus
user_in.reg_strobe	1	Output	Register space access strobe signal; indicates a valid register space cycle when '1'
user_in.dma_strobe	1	Output	DMA access strobe signal; indicates a valid DMA-To-PE cycle when '1'
user_in.dma_in_progress	1	Output	This signal goes low when all DMA-From-PE data has been transmitted to the host.
user_in.write	1	Output	Write select interface signal; indicates a write cycle when '1' or a read cycle when '0' (when strobe is '1')
user_in.pci_rdy	1	Output	Set to '1' when the PCI controller can accept DMA data
user_in.bus_gnt	1	Output	Set to '1' when the PE can master the LAD bus
user_in.reset	1	Output	PE Reset Signal. Can be toggled by a host API call
user_in.rxcclk_in	1	Output	PCI to PE transmit clock DLL input signals.
user_out.data_out	32	Input	User interface to the output data to the LAD bus
user_out.strobe_out	1	Input	The PE drives this signal to '1' during DMA Init, DMA-From-PE and register read LAD bus cycles to indicate that the requested data has been driven on the LAD bus.
user_out.dma_init	1	Input	The PE drives this signal during a DMA initialization cycle.
user_out.pe_rdy	1	Input	'1' indicates that the PE can accept DMA data '0' indicates that the PE cannot accept DMA data
user_out.int_req	1	Input	User interface to the interrupt request signal; Driving this line high for >90ns will create an interrupt to the host.
user_out.bus_req	1	Input	The PE drives this signal to '1' to request LAD bus mastering. The PCI controller will respond by setting User_In.BusGnt to '1' when mastering is possible.

7.1.3 IO Connector Interface (io_connector_interface)

The IO connector is the primary means of communicating with the mainboard. The IO connector contains 79 differential IO pairs for the PRO 1.5GHz A/D I/O card to communicate with the mainboard

The component declarations for the `io_connector_interface` and port record types are shown below:

```

component io_connector_interface is
port (
  pads          : inout io_connector_pads_type;
  reset         : in std_logic;
  reserved      : inout io_reserved_type;
  user_in       : out io_connector_interface_in_type;
  user_out      : in io_connector_interface_out_type
);
end component;

```

```

type io_connector_interface_in_type is record
  rx_clock_in   : std_logic;
  data_in       : std_logic_vector (78 downto 0);
end record;

```

```

type io_connector_interface_out_type is record
  data_out      : std_logic_vector (78 downto 0);
  data_oe_out   : std_logic_vector (78 downto 0);
end record;

```

The “pads” signals of the `io_connector_interface` component are only used to connect the `io_connector_interface` component to the pads, and should always be assigned to `pads.io_connector`.

A definition of each of the port signals is given in Table 7-3 below.

Table 7-3: IO Connector Interface Component Port Signals

Signal Name	Width	Dir	Description
pads	NA	Bi-dir	IO Connector Pad signals
reset	1	Input	Global reset (or set) signal; connected to the GSR input of a STARTUP_Virtex component
Reserved	NA	Bi-dir	Reserved signals
user_in.rx_clock_in	1	Input	Receive clock from IO Connector
user_in.data_in	79	Input	Receive data from IO Connector
user_out.data_out	1	Output	Transmit data to IO Connector
user_out.data_oe_out	1	Output	Controls direction of data. ‘1’ → Output ‘0’ → Input

7.1.3.1 Reserved Registers

Three permanent registers are built into the PRO 1.5GHz A/D I/O card VHDL model and are located at the beginning of the address map for the main I/O PE.



INFORMATION NOTE

A full block of address space for the I/O PE is blocked off for internal use. This space goes from 0x00 to 0x3C on the PE. Registers should not be created in these locations.

Below are descriptions of each register:

Version Register (0x0): This register contains the VHDL version. Bits 23 to 16 contain the major release number. Bits 15 to 8 contain the minor release number, and Bits 7 to 0 contain the second minor release number.

DCM Control Register (0x02): This register controls most of the PE's clock DCMs. The example source (C and VHDL) included shows how to use this register. Table 7-4 describes its contents.

BPE Serial Data Register 0 Write (0x10): This register contains the lower 32 bits of data to be written across the serial interface to the BPE. A subsequent write to the Serial Configuration Control Register is required to start the write transaction. Table 7-5 describes the contents of the 64-bit serial data register.

BPE Serial Data Register 1 Write (0x11): This register contains the upper 32 bits of data to be written across the serial interface to the BPE. A subsequent write to the Serial Configuration Control Register is required to start the write transaction. Table 7-5 describes the contents of the 64-bit serial data register.

BPE Serial Data Register 0 Read (0x12): This register contains the upper 32 bits of the data received on the last BPE serial bus read access. Table 7-5 describes the contents of the 64-bit serial data register.

BPE Serial Data Register 1 Read (0x13): This register contains the upper 32 bits of the data received on the last BPE serial bus read access. Table 7-5 describes the contents of the 64-bit serial data register.

BPE Serial Bus Configuration Control Register (0x14): This register is used to initial BPE serial bus reads and writes and to configure various BPE controls. Table 7-6 describes its contents.

Signature Register (0x3C): This register is reserved by the software as a test register only.

Table 7-4: Description of DCM Control Register

Bit	R/W	Default	Description
31-5	R	0	Reserved
4	R	0	Receive Clock DCM Locked
3	R	0	P Clock DCM Locked
2	R	0	Reserved
1	R/W	0	P Clock DCM Clock Output Enable
0	R/W	0	P Clock DCM Reset

Table 7-5: Description BPE Serial Data Register

Bit(s)	R/W	Default	Description
63-62	R	00	Reserved
61	R/W	0	Reserved : Must be kept 0
60-51	R	0000000000	Reserved
50-32	R	0x00000	CLOCK FREQUENCY: 19-bit unsigned value representing 1/16 th of the current measured sample clock rate, in kilohertz. This field is continuously updated every 1 millisecond.
31-24	R/W	0x00	NEWPS: 8-bit signed value representing a number between -128 and 127 and indicating the phase shift which should be applied to the ADC clock DCMs in the BPE. Writing a new value to this register will result in a DCM adjustment and clearing of the PSDONE bit. When the adjustment is complete, the PSDONE bits will be set.
23-16	R	0x00	CURRENTPS: 8-bit signed value indicating the phase shift currently being applied to the ADC clock DCMs in the BPE.
15	R	0	Reserved
14	R	0	PSDONE: '0' when the ADC clock DCM is adjusting to a new phase shift. '1' when the ADC clock DCM has finished adjusting to a new phase shift.
13-10	R	0000	Reserved
9	R	0	ADCLOCK: '1' when the ADC clock in the BPE is locked.
8	R	0	PCLKLOCK: '1' when P clock in the BPE is locked
7	R	0	Reserved

Bit(s)	R/W	Default	Description
6	R	0	-5VPWRGD: '1' when the ADC's -5V power supply is within acceptable range.
5-4	R	01	BPE version number upper bits.
3-0	R	0001	BPE version number lower bits.

Table 7-6: Description of BPE Serial Bus Configuration

Bit	R/W	Default	Description
31-14	R	0x00000	Reserved
13	R/W	0	External Clock Select: Set to '1' to use an external ADC sample clock. Set to '0' to use an onboard oscillator, when applicable.
12	R/W	0	BPE Push Enable: Set to '1' to enable ADC sample data to be sent to the PE ADC interface.
11	R	X	P Clock Locked: '1' when the BPEs P Clock DCMs are locked.
10	R	X	ADC Clock Locked: '1' when the BPEs ADC Clock DCMs are locked.
9	R/W	0	P Clock Reset: Set to '1' to hold the BPE's P Clock DCM in reset.
8	R/W	0	P Clock Reset: Set to '1' to hold the BPE's ADC Clock DCM in reset.
7	R/W	0	ADC Trigger Select: Set to '1' to select the PE to drive the ADC trigger. Set to '0' to select the external ADC trigger input to drive the ADC trigger.
6	R/W	0	PE Trigger: PE driven trigger output.
5	R/W	0	ADC Clock Enable: Set to '1' to enable the ADC sample clock. Set to '0' to shutdown the ADC and disable to sample clock. NOTE: This bit must be asserted during all serial data register transactions, however it should be de-asserted when the ADC is not in use.
4	R	0	Reserved
3	R	X	1.5V Power Good: '1' when the 1.5V supply is within acceptable range.
2	R	0	Read Complete: '1' when the last read request is completed. This must be used in conjunction with the Serial Access bit to determine when a read access request has completed. The read is complete when Serial Access is '0' and Read Complete is '1'.
1	R/W	0	Serial Access: Set to '1' to start a serial read or write access. This bit is cleared to '0' automatically when the read or write access has started. This must be used in conjunction with the Read Complete bit to determine when a read access request has completed. The read is complete when Serial Access is '1' and Read Complete is '1'.
0	R/W	0	Access Type: Set to '1' to select a serial write access. Set to '0' to select a serial read access. The access is not started until the Serial Access bit is set.

7.1.4 IO DRAM Portx Interface (dram_portx_interface)

The io_dram_portx_interface provides the user interface for DRAM.

The IO DRAM portx interface is defined as:

```

component io_dram_portx_interface is
generic (
    DRAM_SIZE      : natural := 256
);
port (
    pads           : inout io_dram_pads_type;
    reset          : in std_logic;
    reserved       : inout io_reserved_type;
    p_clock        : in io_clock_in_type;
    ref48_clock    : in std_logic;
    user_in        : out io_dram_interface_in_type;
    user_out       : in io_dram_interface_out_type
);
end component;

```

The io_dram_portx_interface_in_type is defined as:

```

type io_dram_interface_in_type is record
    data_in          : std_logic_vector(127 downto 0);
    data_in_available : std_logic;
    write_rdy        : std_logic;
    read_rdy         : std_logic;
end record;

```

The io_dram_portx_interface_out_type is defined as:

```

type io_dram_interface_out_type is record
    addr           : std_logic_vector(24 downto 0);
    data_out       : std_logic_vector(127 downto 0);
    data_in_ce     : std_logic;
    write          : std_logic;
    read           : std_logic;
end record;

```

The port signals of the DRAM interface are shown in the following table.

Table 7-7: IO DRAM portx Interface Component Port Signals

Signal Name	Width	Dir	Description
reset	1	Input	Global reset (or set) signal
p_clock	1	Input	Input Clock. All data bits are synchronous to this clock.
ref48_clock	1	Input	Input reference clock. Should connect to ref48_clock
pads	NA	Bi-Dir	DRAM Pad signals
user_out.data_out	128	Input	User Data to be outputted by DRAM
user_out.data_in_ce	1	Input	Read Data FIFO CE to receive read data from DRAM
user_in.data_in	128	Output	Data from the DRAM to the user
user_in.data_available	1	Output	Signifies that output data is available in read data FIFO
user_out.write	1	Output	User Write control signal
user_out.read	1	Output	User Read control signal
user_in.write_rdy	1	Output	User Write Ready signal
user_out.read_rdy	1	Output	User Read Ready signal
user_out.addr	25	Output	User Strobe control signal

To write data to the SDRAM, first check that the 'write_rdy' signal is high. This step ensures that the write FIFOs are not full. If 'write_rdy' is high, the interface is ready to accept write data. Next, put the address on the 'addr' lines and the 128-bit data on the 'data_out' lines and then pulse 'write'. Data can be sent in continuously as long as 'write_rdy' is high.

To read data back, first check that 'read_rdy' is high to make sure that the read address FIFOs are not full. Then, put the address on the 'addr' lines and pulse 'read'. Again, the address of data to be read can be continuously written into the interface as long as 'read_rdy' is high. Soon afterwards, the 'data_available' signal goes high. This data waits in a read FIFO.

To access the data, pulse 'data_in_ce'. Once this is done, the 128-bit read data will be available on the 'data_in' lines.

7.1.5 IO ADC Interface (io_adc_interface)

The ADC interface provides access to the onboard analog to digital converter data via the BPE.

The io_adc_interface is defined as:

```
component io_adc_interface is
generic (
    REVISION : string := "B"
);
port (
    pads           : inout io_adc_pads_type;
    reset          : in std_logic;
    reserved       : inout io_reserved_type;
    p_clock        : in std_logic;
    rx_clock       : in std_logic;
    ref48_clock    : in std_logic;
    user_in        : out io_adc_interface_in_type;
    user_out       : in io_adc_interface_out_type
);
end component;
```

The io_adc_interface_in_type is defined as:

```
type io_adc_interface_in_type is record
    data_in           : std_logic_vector (143 downto 0);
    data_available    : std_logic;
end record;
```

The io_adc_interface_out_type is defined as:

```
type io_adc_interface_out_type is record
    data_in_ce       : std_logic;
end record;
```

Once the ADC has been set up and enabled by LAD writes to the BPE reserved registers, the IO ADC interface will start collecting data. The IO ADC interface parallelizes the incoming data into 16 sample + trigger pairs for a total of 144 bits. Each 144 bit word is presented synchronous to P Clock. When the interface has collected enough data, user_in.data_available is set to one '1', and the PE design can then accept the data. To accept the data set user_out.data_in.ce to '1'.

The data is then driven on user_in.data in on the following rising edge of p_clock. User_out.data_in_ce may be kept high as long as user_in.data_available is high.

The 144 data bits contain a combination of sampled data and trigger values. The mapping of these bits is shown in the table below.

Table 7-8: ADC Interface Data Mapping

Bit(s)	Description
143	Sample (n+15) Trigger
142-135	Sample (n+15)
134	Sample (n+14) Trigger
133-126	Sample (n+14)
.	.
.	.
.	.
17	Sample (n+1) Trigger
16-9	Sample (n+1)
8	Sample n Trigger
7-0	Sample n

7.1.6 IO LED Interface (io_led_interface)

The LED interface provides access to the three light emitting diodes (LEDs) on the PRO 1.5GHz A/D I/O card. The LEDs can be used to indicate status or processing activity, or to help debug a PE design.

The io_led_interface is defined as:

```

component io_led_interface is
port (
    pads          : inout led_pads_type;
    reset         : in std_logic;
    clock         : in std_logic;
    user_out      : in io_led_interface_out_type
);
end component;

```

The io_led_interface_out_type is defined as:

```

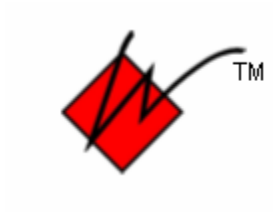
type io_led_interface_out_type is record
  red          : std_logic;
  yellow       : std_logic;
  green        : std_logic;
end record;

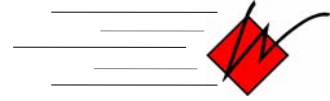
```

The port signals of the LED standard interface are shown below. The user_out signals should be used to drive the LEDs of the PE device.

Table 7-9: LED Interface Component Port Signals for non-ACE

Signal Name	Width	Dir	Description
pads	3	Output	LED pad signals
user_out.red	1	Input	User interface to the red LED, '1' = ON
user_out.green	1	Input	User interface to the green LED, '1' = ON
user_out.yellow	1	Input	User interface to the Yellow LED, '1' = ON





8. WILDSTAR™-II VHDL DESIGN CYCLE

The WILDSTAR™-II VHDL design cycle consists of several simple steps that help you create, simulate, synthesize, and analyze a WILDSTAR™-II system design. This chapter describes how to create a design using the WILDSTAR™-II and system VHDL models.

8.1 WILDSTAR™-II /VME and /PCI VHDL Design

8.1.1 Using Template VHDL Design Files

Template files should be used when creating a WILDSTAR™-II design, since the template files have been pre-designed to contain most of the boilerplate interface logic needed by every design. Starting from scratch would not only take much longer, but would also increase the risk of implementing interface logic that is incorrect or incomplete.

The following VHDL template files are all found in the sub-directory called “\$ANNAPOLISII_BASE/ad15ghz_pro_io_card/template/sim” (where \$ANNAPOLISII_BASE is the installation path of your mainboard VHDL, and should be copied to a design project directory and used as a starting point for the design:

Table 8-1: VHDL Template Files

project_vcom.do	Modeltech® macro script file
project_vsim.do	Modeltech® macro script file
host_template_arch.vhd	Host design template architecture
pe_template_arch.vhd	PE0/PE1 design template architecture
pe_revb_template_arch.vhd	PE0/PE1 design template architecture (Rev B boards only)
pe2_template_arch.vhd	PE2 design template architecture.
system_template_arch.vhd	System template architecture.
system_cfg.vhd	System design configuration

8.1.2 Creating a PE Design

The PE template file should be modified by removing the comments from the standard interfaces needed by the design. The user-defined portion of the application should be made to reside in a separate component and file. Hierarchical design should be used in order to keep the complexity of any single component to a minimum.

8.1.3 Creating a Host Design

Commands such as WSII_WriteRegs_32 or WSII_ReadRegs_32 can be issued to the ModelSim® simulator by using VHDL to create a host model.

8.1.3.1 Using the VHDL Host Template

The host template file should be modified by removing the comments from the API procedures and modifying the program flow to suit the design. The host program usually resides in a single sequential main process, but it is possible to mimic a “multi-threaded” program by having more than one process. Currently, however, a lock or a mutual exclusion mechanism must be built for issuing commands to the PCI Controller.

8.1.4 Creating a System Architecture

The template system architecture file, `system_template_arch.vhd`, creates a system with only one board, labeled “board zero”. To add more boards to the system, uncomment the desired number of board architectures and their corresponding command processing lines in the `P_CMD` process in the `system_template_arch.vhd` file.

8.1.5 Modifying Configuration Files

The system configuration (`system_cfg.vhd`) file must also be modified to meet the needs of the design. Model details such as memory bank type, PE architecture, and host architecture can be set inside this configuration file. Simply follow the instructions inside the configuration file on how to change the user-modifiable portions of the WILDSTAR™-II VHDL model.

8.1.6 Design Simulation

This section discusses how to simulate a WILDSTAR™-II VHDL design using the Model Technology, Inc., ModelSim® VHDL simulator.

8.1.6.1 Compiling the UNISIM library

The UNISIM library provides a simulation model for the various Xilinx® Virtex-II primitives used in the VHDL model. This library must be compiled once before your first simulation.

Xilinx provides the executable “`complib`” to compile the UNISIM library for various platforms. To compile the UNISIM library for the WILDSTAR™-II, use the following parameters:

- `-w` : To overwrite any existing compiled files
- `-f virtex2:u` : To select the Virtex™-II UNISIM library
- `-l vhdl` : To select VHDL as the target language
- `-o <Annapolis base>|<board>|vhdl`: To set the target output directory. Set <Annapolis Base> to you root Annapolis directory

(typically c:\annapolis), and <board> to wsii_vme or wsii_pci for WILDSTAR™-II/VME or WILDSTAR™-II/PCI respectively.

- **-s <mti_se/mti_pe>** : To select the simulator. Use *mti_se* for ModelSim SE versions and *mti_pe* for ModelSim PE.
- **-p <path>** : To set the path to the ModelSim program. <Path> is the directory where the ModelSim executable is located.

For example, to compile the UNISIM library for a WILDSTAR™-II/VME, the following command might be used:

```
compplib -w -f virtex2:u -l vhdl -s mti_se -p  
c:\ModelTech5.7\win32 -o c:\annapolis\wsii_vme\vhdl
```

8.1.6.2 Using Template ModelSim® Macro Files



INFORMATION NOTE

To ensure that all ModelSim® templates are current, the *refresh.do* script should be run (located in the annapolis\wsii_pci\template\sim directory). This script updates all the precompiled libraries shipped with the WILDSTAR™-II VHDL model. If you have installed VHDL in a directory other than <annapolis>, you will need to change the ANNAPOLIS_BASE variable in the *refresh.do* script to point to the proper directory.

The following ModelSim® template files are all found in the sub-directory called “\$ANNAPOLISII_BASE/<Board>/template/sim” (where \$ANNAPOLISII_BASE is the installation path to the WILDSTAR™-II /VME or WILDSTAR™-II /PCI VHDL model and <Board> is either “wsii_pci” or “wsii_vme”), and should be copied to a design project directory and used as a starting point for the design:

project_vcom.do

Project VHDL compilation macro for ModelSim®

project_vsim.do

Project VHDL simulation macro for ModelSim®

Once the macro files have been copied, they should be modified to meet the needs of the design project. Simply follow the step-by-step instructions located inside each of the macro files to customize them for the current design project.

8.1.6.3 Compiling a VHDL Design

Once the macro files have been configured, the design can be compiled using the ModelSim® tool. Follow these simple steps to compile the design:

1. Start the ModelSim® tool
2. In the **Tools** menu (versions 5.6 and newer), select the **Execute Macro...** option.
3. Using the file browser, locate the design project directory.
4. Select the **project_vcom.do** compilation macro file.
5. Click on the **Open** button.

At this point, the compilation messages will begin to scroll in the **ModelSim** window (or **Transcript** window in ModelSim v4.7 or older). If any errors occur during compilation, the error message(s) will also appear in the **ModelSim/Transcript** window.

Once the errors are corrected, repeat steps 1 through 5 above until the design has been completely compiled.

8.1.6.4 Simulating a VHDL Design

Once the VHDL design has been compiled, the design can be simulated using the ModelSim® tool. Follow these steps to simulate the design:

1. Start the ModelSim® tool
2. In the **Tools** menu (versions 5.6 and newer), select the **Execute Macro...** option
3. Using the file browser, locate the design project directory
4. Select the **project_vsim.do** compilation macro file
5. Click on the **Open** button

At this point, the loading messages begin to scroll in the **ModelSim** window (or **Transcript** window in ModelSim® Version 4.7 or older). If any errors occur during the loading of the design, the error message(s) will also appear in the **ModelSim/Transcript** window.

Once the errors are corrected, repeat steps 1 through 5 above until the design has been completely loaded and is ready for simulation. Refer to the ModelSim® manual for details on how to run the simulation.

8.1.6.5 Using Template Synplify® Project Files

The following Synplify® project files are found in the sub-directory called “\$ANNAPOLISII_BASE/<Board>/template/syn” (where \$ANNAPOLISII_BASE is the installation path to the WILDSTAR™-II /VME or WILDSTAR™-II /PCI VHDL model and <Board> is either “wsii_pci” or

“wsii_vme”). The file should be copied to a design project directory and used as a starting point for the design:

pe\pe.prj	PE0/PE1 project VHDL synthesis project file for Synplify®
pe2\pe2.prj	PE2 project VHDL synthesis project file for Synplify®

Once the PE project file has been copied, it should be modified to meet the needs of the design project. Simply follow the step-by-step instructions located inside the project file to customize it for the current design project.

8.1.6.6 Setting up Synthesis Constraints

Certain design constraints can be configured using the Synplify® synthesis tool. Some of these constraints are located at the end of the Synplify® project file. Other design constraints may be added directly to the VHDL code as VHDL attributes, while others can be added to the Synplify® design constraints file (*.sdc). Refer to the Synplify® manual for more information regarding synthesis design constraints.

8.1.6.7 Synthesize the Design

Once the Synplify® project file and design constraints have been configured, the PE design can be synthesized. Follow these steps to synthesize the PE design:

1. Start the Synplify® tool.
2. Close any project window that might be open.
3. In the **File** menu, select the **Open Project...** option.
4. Using the file browser, locate the design project directory.
5. Select the **pe.prj** or **pe2.prj** Synplify® project file.
6. Click on the **Open** button.
7. Click on the **RUN** button.

At this point, compiling and mapping messages begin to appear in the project window. If any warnings or errors occur during the loading of the design, the error indicator will also appear in the project window. Click on the View Log button to review the warning and/or error messages.

Due to the comprehensive nature of the WILDSTAR™-II PE model, you will undoubtedly encounter warnings during the synthesis process. These warnings are usually related to PE I/O signals that are simply unused by the current design project. As a rule, you can ignore any warnings that do not appear in your own design files.

Once the errors (and user warnings) are corrected, repeat steps 1 through 7 above until the design has been completely loaded and is ready for place-and-route. Refer to the Synplify manual for more details on how to use the Synplify® tool.

8.1.6.8 Using Template Makefiles

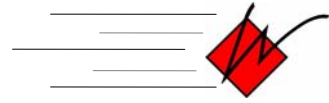
The following Xilinx® Alliance Series makefile files are found in the sub-directory called “\$ANNAPOLISII_BASE/<Board>/template/syn” (where \$ANNAPOLISII_BASE is the installation path to the WILDSTAR™-II /VME or WILDSTAR™-II /PCI VHDL model and <Board> is either “wsii_pci” or “wsii_vme”) and should be copied to a design project directory and used as a starting point for the design:

pe\makefile	PE0/PE1 project makefile for Xilinx Alliance tools
pe2\makefile	PE2 project makefile for Xilinx Alliance tools

Once the makefile has been copied, it should be edited so that the ANNAPOLISII_BASE macro properly reflects the WILDSTAR™-II installation directories. Be sure to use forward slashes (/) in the path name, even if using an operating system that usually requires backslashes in a path name.

Several other variables must be modified in order for the makefile to produce the correct binary file for WILDSTAR™-II.

1. **DEF_PART**: must be set to match the PE part type.
2. **DEF_SPEED**: should be set to match the speed grade of the PE. *If the speed grade does not match, erroneous timing reports will be generated.*



APPENDIX A: SAMPLE PLOTS

Below are sample plots representative of those accompanying each PRO GHz A/D I/O card, with frequency measurements in MHz.

