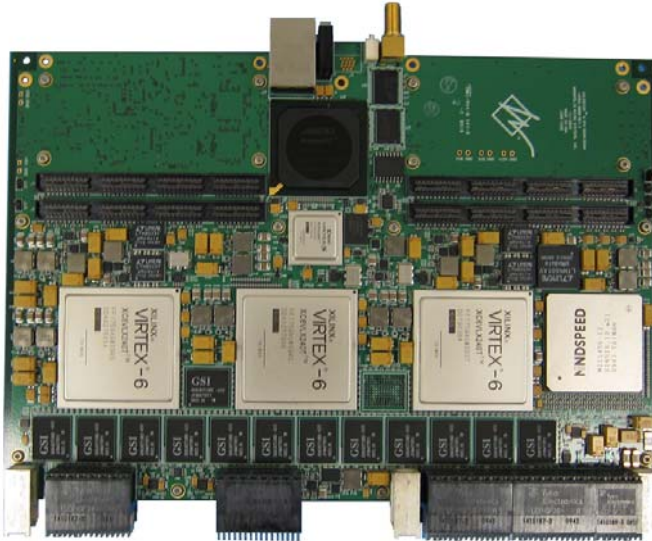


Data Sheet  
Doc # 14379-0000 Rev 1.2

# Annapolis Micro Systems, Inc.

## WILDSTAR™ 6 VPX Card

### Virtex™ 6 Based Processor Board



VIRTEX<sup>6</sup>

OpenVPX™

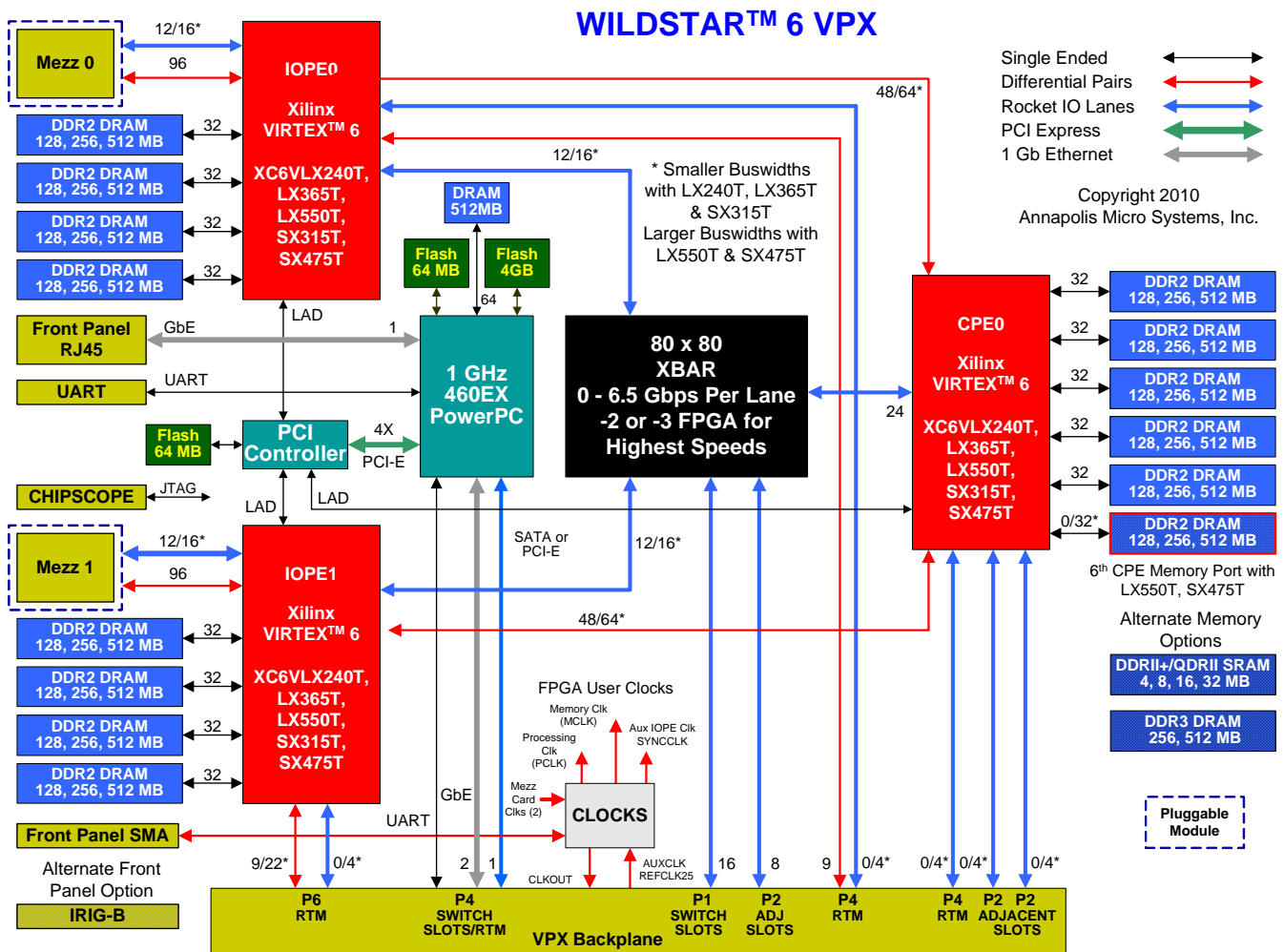


### Features

- Up to Three Virtex™ 6 FPGA Processing Elements
  - XC6VLX240T, LX365T, LX550T, SX315T, or SX475T
- Up to a Board Total of 3.1 GB DDR2 DRAM, 3.1 GB DDR3 DRAM or 192 MB DDRII+ or QDRII SRAM in 5 or 6 Memory Banks for the Computational FPGA on Board
- Up to a Board Total of 4 GB DDR2 DRAM, 4 GB DDR3 DRAM or 256 MB DDRII+ or QDRII SRAM Arranged in 4 Memory Banks for each of Two IO FPGAs on Board
- On Board Host AMCC 460EX PowerPC with Clock Speeds up to 1GHz
- 512 MB DRAM for PowerPC
- 64 MB NOR FLASH
- 4 GB NAND FLASH to Store FPGA Images and for Application Data
- 4X PCI Express Gen 1 Between PPC and PCI Controller
- Host Software : Linux, VxWorks - API and Device Drivers
- Full CoreFire™ Board Support Package for Fast and Easy Application Development
- Open VHDL Model including Source Code for Hardware Interfaces and ChipScope Access
- Open VHDL IP Package for Communication Interfaces
- Current, Voltage and Temperature Monitoring Sensors via API Software Interface
- Accepts Standard Annapolis WILDSTAR 4 / 5 / 6 Family I/O Modules
- Quad 130 MSps thru Quad 550 MSps A/D, 1.5 GSps thru 2.2 GSps A/D, 5.0 GSps A/D
- Quad 600 MSps D/A, Dual 1.5 GSps thru 4.0 GSps D/A
- Infiniband, 10G Ethernet and SFPDP
- Integrated Heat Sink
- Full IPMI Chassis Management Support



Made in the USA



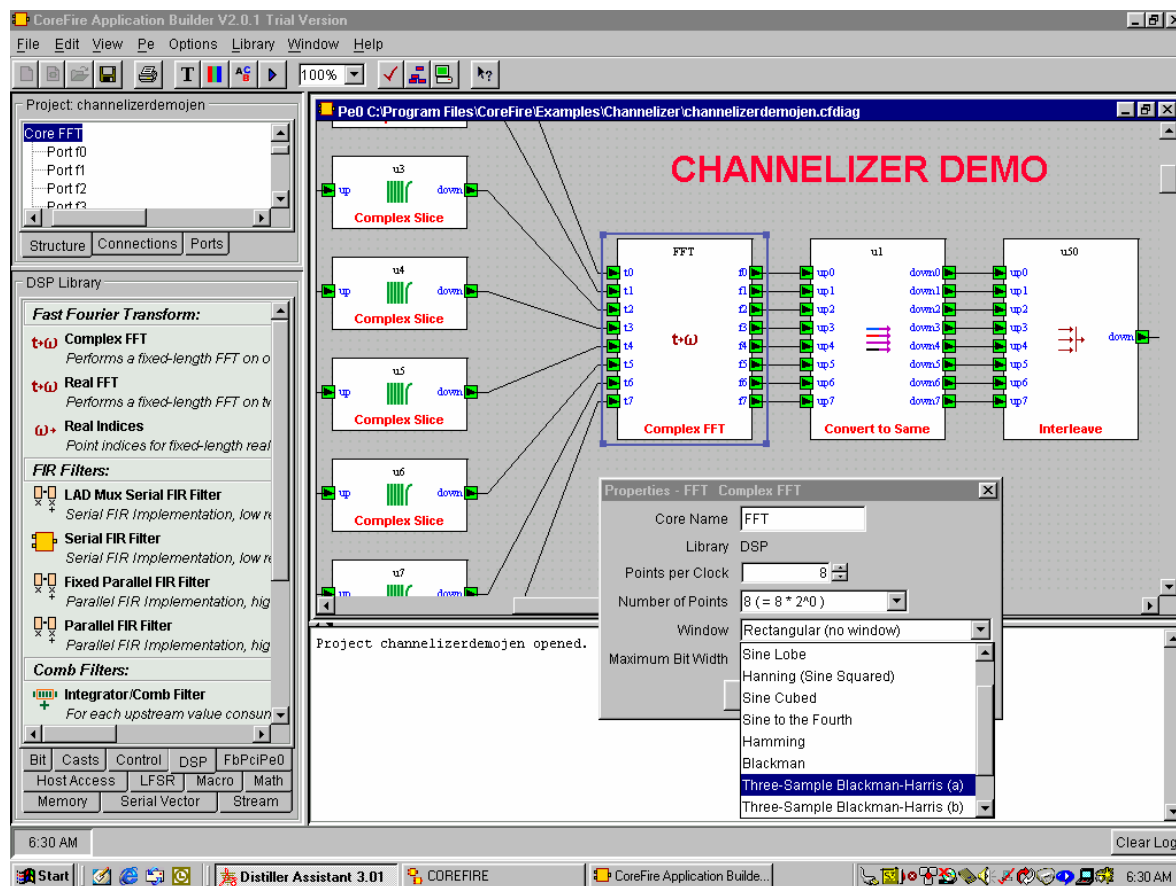
## Benefits

- Reduce Risk With Our 14th Generation of COTS (Commercial Off the Shelf) FPGA Based Processing Boards
- Annapolis is Already Delivering Virtex 6 PCI-Express Products and Blade Pluggable Modules
- Annapolis Understands and Has Already Solved any Virtex 6 Issues
- Save Time and Effort - Develop Your Application Very Quickly and Easily with CoreFire™
- CoreFire™ Provides Proven, Reusable, High Performance IP Modules, Including Some of the World's Fastest FFTs and Filters
- VHDL Users Supplied with Source Code for Hardware Interfaces and ChipScope Access
- VHDL IP Package Includes Communication Interfaces
- Standardize and Control Your Team's Development
- Achieve World Class Performance
- WILD™ Solutions Outperform the Competition
- Training Classes and Application Support

## Debug and Maintenance

- Access JTAG and Use ChipScope via Front Panel
- Product Includes Full BIST (Built In Self Test Software)

# CoreFire™ Ready - Create and Run Designs on Day 1



All WILDSTAR™ 4 / 5 / 6 boards are fully compatible with the CoreFire™ Design Suite, an FPGA design application tool developed by Annapolis Micro Systems, Inc.

The CoreFire™ Design Suite is a Graphical User Interface (GUI) tool using Data Flow Methodology which combines Annapolis's extensive systems and application development experience with their large collection of tightly crafted high performance Intellectual Property (IP) Cores, the automatic generation of the logic necessary to control the interfaces between the modules, and Hardware in the Loop Debugging to provide an exceedingly convenient and fast methodology for developing FPGA application files. With CoreFire™ it is possible to completely implement an algorithm on our WILD™ Family of Field Programmable Gate Array (FPGA) boards without ever descending to the lower level hardware details, saving months of development time and money.

FPGA designers who have in the past struggled for months to develop applications using VHDL are finding that CoreFire™ enables them to achieve better FPGA performance in a fraction of the time.

Combined with the Annapolis COTS WILDSTAR™ 4 / 5 / 6 FPGA boards with many million gates in each slot, using Xilinx Virtex™ 4, Virtex™ 5 and Virtex™ 6, the power of CoreFire™ can automatically and quickly provide correct, reconfigurable and reliable FPGA designs for these boards. Real world application experience has shown CoreFire™ to be the critical tool that enables the timely development of highly specialized FPGA designs, ensuring each program's success.

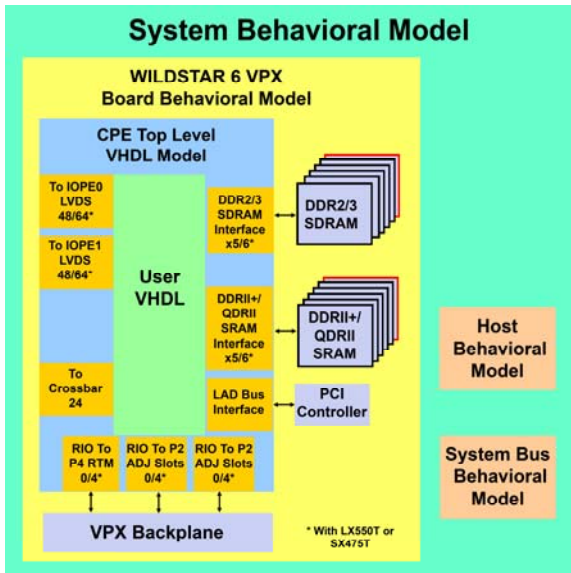
Gone are the days when an Application Developer had to learn hardware design methodologies, such as VHDL, Verilog, or low level schematic entry. CoreFire™'s "drag and drop" approach keeps the User operating on the conceptual, data flow level of his problem throughout the whole development process so he can concentrate on solving problems, not on designing hardware.

## WILDSTAR 6 VHDL HW Interfaces (Full Source Code Provided)

- LAD Bus
- DMA Bus
- DDR2 SDRAM
- DDRII/QDRII SRAM
- Rocket I/O Mezzanine Interface
- LVDS I/O Mezzanine Interface
- Interfaces between FPGAs
- High Speed Rocket I/O to Backplane
- Basic Board Functions - Clocks, Reset, LEDs

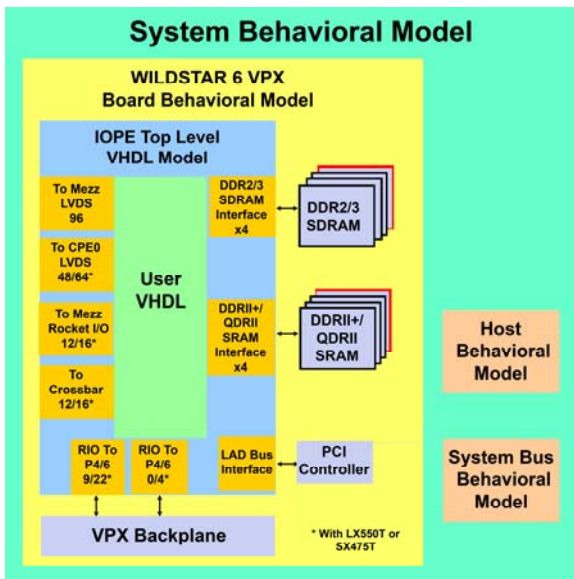
## WILDSTAR 6 VHDL IO Communication Interfaces (Encrypted Cores Provided)

- 1 GbE
- 4x PCI-E Gen 2



## FPGA VHDL Template

- User VHDL is instantiated into the provided PE top level VHDL model
- User manually includes the supplied Annapolis physical interfaces
- User writes VHDL code to interface to the Annapolis interfaces



## Abstract Chip Level Interfaces

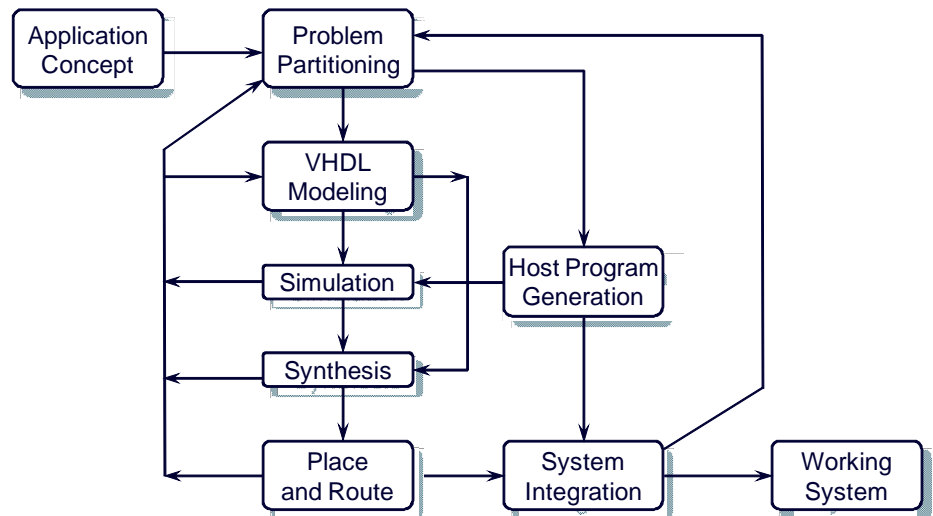
- Physical pad locations are available and accessible by the developer, but are abstracted within the VHDL model for ease of use
- Abstract tri-state control of bidirectional buses
- Simplify multi-cycle interfaces to single cycle operations
- De-multiplex multiplexed bus interfaces
- Optimized clocking scheme

## WILDSTAR 6 Host Software

- Allows Host System access to the WILDSTAR 6 Board
- C API Function Call to interact with System
- C API Function Calls to Configure Board
- C API Function Calls to Transfer Data

## Driver API Function Call Modules

- Clock - Provides access to WILDSTAR 6 clocks
- Direct Memory Access (DMA) - Provides interface between the PPC and on board memory
- Error - Monitors and queries API errors
- Ethernet APIs - Perform Ethernet functions
- General - Allows a WILDSTAR 6 board to be detected and initialized
- Information Access - Provides access to information from various sources
- Interrupt Handling - Provides access to Interrupts and Interrupt Handling
- Processing Element (PE) - Provides interface to configure and program WILDSTAR 6 PE
- Register Access - Provides access to the register space of WILDSTAR 6 PE
- Sensor - Provides access to board sensors
- XML Description - Allow direct access to hardware descriptions in XML format
- API Function Calls to Configure Board



## **WILDSTAR 6 VHDL Support Tools**

- Simulation - Mentor Graphics ModelSim
- Synthesis - Synplicity Synplify Xilinx XST
- Place and Route - Xilinx

## **Annapolis VHDL Hardware Interface Models**

- Optimized for best performance and lowest latency.
- Provide fully tested interfaces to drastically reduce customer design iterations
- Full open source, for maximum visibility and access by the developer

## **WILDSTAR 6 VHDL Design Methodology**

- Write VHDL user code for PE using provided template
- Connect VHDL user code up to provided user interfaces (LAD bus, DMA, DRAM, etc.)
- Simulate design using included ModelSim scripts and verify its functionality using VHDL "host code" templates to simulate software API calls
- Synthesize design with Synplify or XST using included script files
- Place and Route design using Xilinx tools using included script files
- Write C code using provided templates to program in compiled PE image and run applicable API calls
- Run the completed FPGA file on the WILDSTAR 6 hardware and the compiled C code on the onboard Host PPC

## **VHDL Model Simulation Environment**

- Behavioral Model of all functional components on WILDSTAR 6 AMC
- Synthesizable Source VHDL of hardware interfaces to all PE accessible components (LAD Bus, DMA, DRAM, etc)
- Individual Source Examples for each hardware interface
- Scripts for simulation, synthesis, and place & route
- Templates for user to develop VHDL PE designs
- Documentation on all of the above
- Support for Mentor Graphics ModelSim, Synplicity Synplify, Xilinx XST, and Xilinx ISE Foundation tools
- Support for Xilinx ChipScope
- System Level Model
  - Simulate the Host Computer, Place Multiple Boards in a System, and arbitrarily interconnect the Boards to each other and to External Sources
- Board Level Model
  - Simulate Board Components - Memories, Buses, I/O Ports
- PE Level Model
  - PE Interfaces and User Logic for driving PE pins
  - Completely synthesizable
- Will eventually become the Bitstream that programs the PE



## **In House Manufacturing**

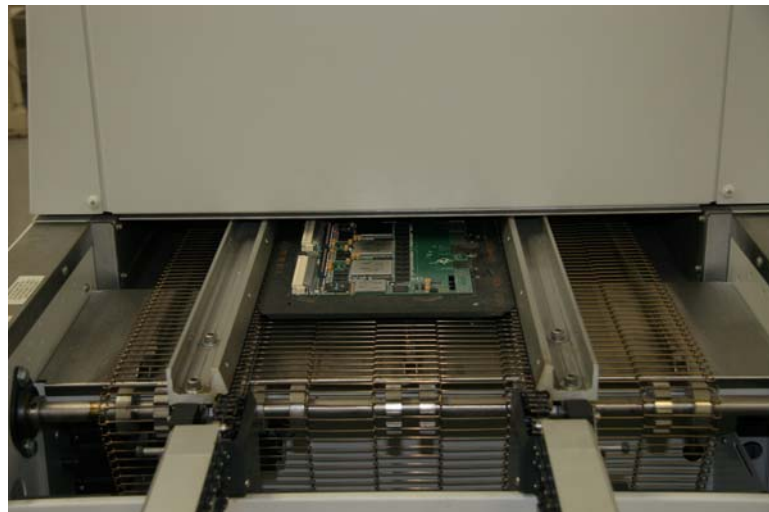
Annapolis has been building and delivering COTS and Custom Software, Hardware and System Products for Fortune 100, Fortune 500 and Government Customers since 1982. We know how to manufacture state of the art high performance boards, and have many years experience successfully producing surface mount products.

The Annapolis Engineering Team has many many years of experience working on the cutting edge of technology.



## **Proactive Thermal and Power Management To Ensure Safe and Reliable Processing**

- Combination Heat Sink/Fans
- Sensors across the board monitor Current, Voltage and Temperature, with automatic warning/shutdown capability to prevent excessive heat buildup
- Individual Power Supply and Management for I/O Slot and for FPGA Processing Element
- All monitoring and control through Host Software
  - Via API Calls
  - Via MMC



## WILDSTAR 6 VPX Part Number Decoding

Build the Part Number				
( WS6 / CPE Type - Speed Grade & Backplane / IOPE Type - Qty - Speed Grade				
/ CPE Memory Size & Type / IOPE Memory Size and Type				
/ SMA Termination / Conformal Coating )				
Sample Part Number				
WS6/XC6LX240T-2VPX/XC6LX240T-2/2.6GD2D/4GD2D/IRIG-B				
Part Number				
WS6/ = WILDSTAR™ 6 - Default = 1 Computational PE				
or WS6Ind/ = WILDSTAR™ 6 Industrial Temperature Range				
Default = 1 Computational PE				
XC6xxxxxx = Virtex 6 FPGA Computational Processing Element (CPE0):				
LX240T, LX365T, LX550T, SX315T, SX475T				
or B- = I/O FPGAs only, no Computational FPGAs				
-x = Speed Grade: -1 = 1C or 1I, -2 = 2C or 2I, -3 = 3C				
xxxx/ = Backplane: VPX = VPX				
XCxxxxxx = Virtex 6 FPGA IO Processing Element (IOPE0 and IOPE1):				
LX240T, LX365T, LX550T, SX315T, SX475T				
or B = Computation FPGA only, No I/O FPGAs				
/xxx= Blank = Default = Both IO FPGAS				
/IO0 = One IO FPGA = PE0, /IO1 = One IO FPGA = PE1				
-x = Speed Grade: -1 = 1C or 1I, -2 = 2C or 2I, -3 = 3C				
/xxxxxxx = Computational PE Memory:				
For LX240T, LX365T and SX315T = 640MD2D, 1.3GD2D, 2.6GD2D, 1.3GD3D,				
2.6GD3D, 20MD2+S, 40MD2+S, 80MD2+S, 160MD2+S,				
20MQ2S, 40MQ2S, 80MQ2S, and 160MQ2S				
For LX550T and SX475T = 768MD2D, 1.5GD2D, 3.1GD2D, 1.5GD3D, 3.1GD3D,				
24MD2+S, 48MD2+S, 96MD2+S, 192MD2+S,				
24MQ2S, 48MQ2S, 96MQ2S, and 192MQ2S				
/xxxxxxx = I/O PE Memory: 512MD2D, 1GD2D, 2GD2D, 4GD2D, 1GD3D, 2GD3D,				
4GD3D, 16MD2+S, 32MD2+S, 64MD2+S, 128MD2+S, 256MD2+S,				
16MQ2S, 32MQ2S, 64MQ2S, 128MQ2S, 256MQ2S				
/xxxxxx = SMA Termination = 0.7VAC, 1.4VAC, 0.7VDC, 1.4VDC or IRIG-B				
/CC = Conformal Coating				
(Note: D2D = DDR2 DRAM, D3D = DDR3 DRAM, D2+S = DDRII+ SRAM, Q2S = QDRII SRAM)				

**Annapolis is famous for the high quality of our products,  
and for our unparalleled dedication to ensuring  
that the customers' applications succeed.**

**We offer training classes and  
exceptional special application development support.**

