Data Sheet
Doc # 14517-0000 Rev 1.2

Annapolis Micro Systems, Inc. WILDSTAR™ 6 for PCI-Express

Virtex™ 6 Based Processor Board

FEATURES

- Up to 3 Virtex™ 6 FPGA Processing Elements
  - XC6VLX240T, LX365T, LX550T, SX315T, SX475T
- Up to 8 GBytes DDRII DRAM in 14 Memory Banks per Board or
- Up to 8 GBytes DDR3 DRAM in 14 Memory Banks or
- Up to 480 GBytes DDRII+ or QDRII SRAM in 15 Banks per Board
- Programmable FLASH to Store FPGA Images
- 8X PCI Express Gen1 or Gen2
- Supports PCI Express Standard External Power Connector
- High Speed DMA Multi-Channel PCI Controller
- Host Software : Windows, Linux - API & Device Drivers
- Full CoreFire™ Board Support Package for Fast, Easy Application Development
- VHDL Model including Source Code for Hardware Interfaces, including ChipScope Access
- Also Available in Industrial Temperature Grades

BENEFITS

- Reduce Risk With Our 15th Generation of COTS (Commercial Off the Shelf) FPGA Based Processing Boards
- Save Time and Effort - Develop Your Application Very Quickly and Easily with CoreFire™
- CoreFire™ Provides Proven, Reusable, High Performance IP Modules, Including Some of the World's Fastest FFTs and Filters
- Standardize and Control Your Team's Development
- Achieve World Class Performance
- WILD™ Solutions Outperform the Competition
- WILDSTAR™ 6 for PCI-E with 1 I/O Card Fits in Single PCI Slot - 2nd I/O Card Uses 2nd Slot
- Accepts 1 or 2 COTS Highspeed WILDSTAR™ 4 / 5 / 6 I/O Cards
- Training Classes and Application Support
- Integrated Heat Sink with Fans

Annapolis is famous for the high quality of our products, and for our unparalleled dedication to ensuring that the customers' applications succeed. We offer training classes and exceptional special application development support.

VIRTEX 6

Annapolis Micro Systems, Inc.

Made in the USA

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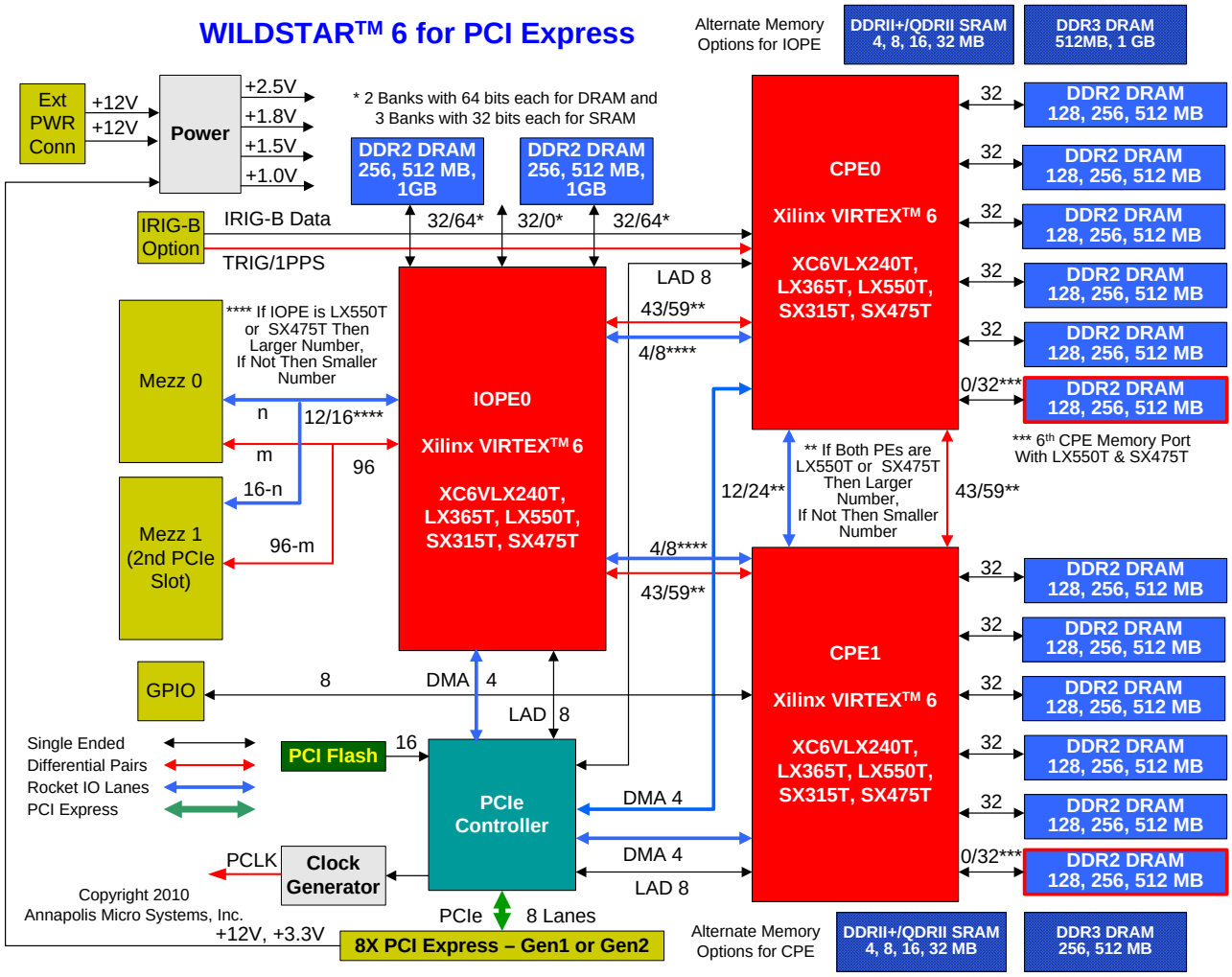


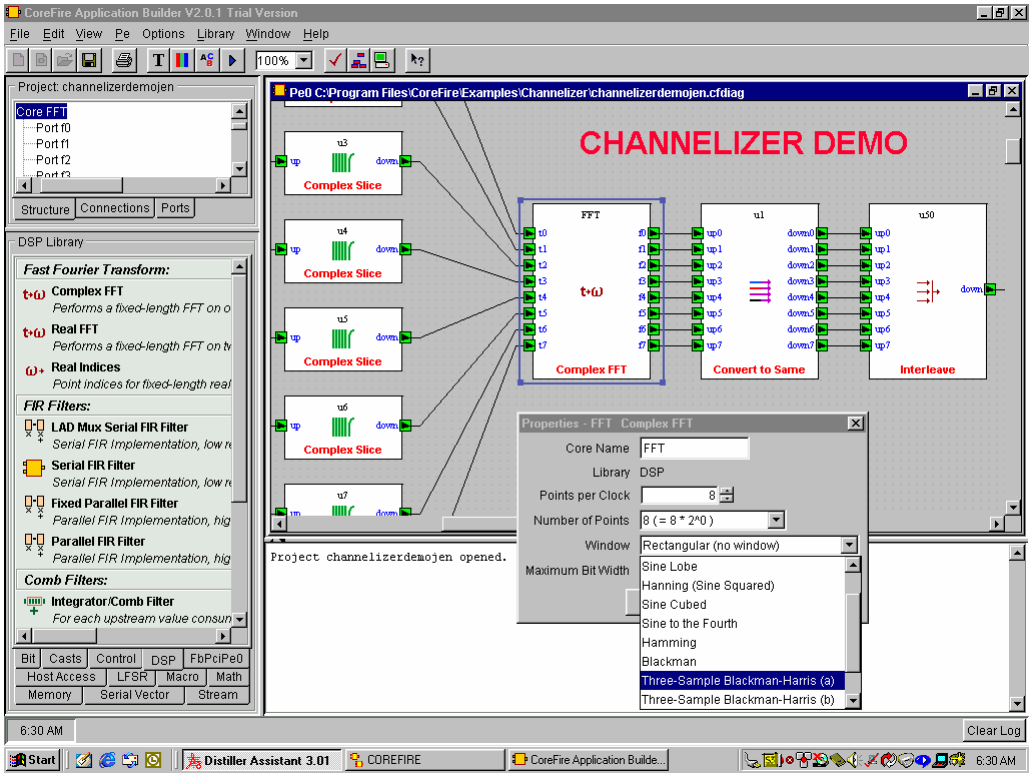
Sample I/O Daughter Cards for WILDSTAR™ 4 / 5 6 Family

Universal 3 Gbit I/O
UNI6

Quad 130 thru Quad 550 MSps A/D
1.5 thru 2.2 GSps A/D
Dual 2.5 or Single 5.0 GSps A/D
Quad 600 MSps D/A
Dual 1.5 GSps thru 4.0 GSps D/A
Infiniband, Rocket I/O, 10G Ethernet

Quad 130 MHz A/D I/O

CoreFire™ Ready – Create and Run Designs on Day 1!



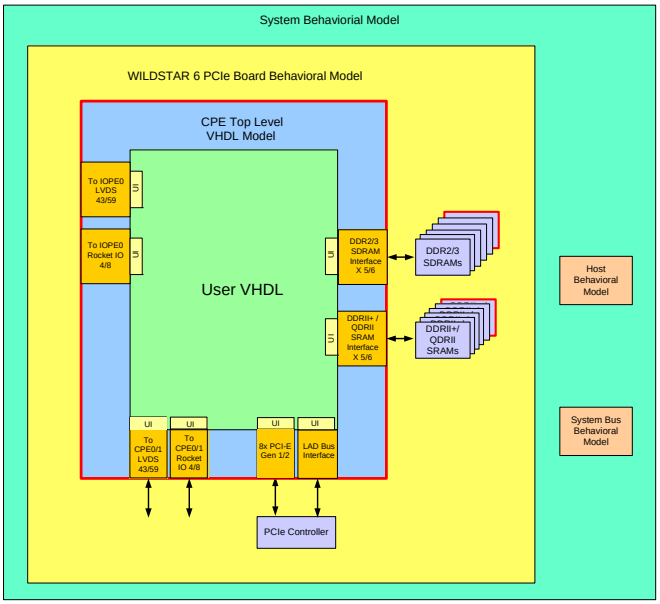
All WILDSTAR™ 4 / 5 / 6 boards are fully compatible with the CoreFire™ Design Suite, an FPGA design application tool developed by Annapolis Micro Systems, Inc.

The CoreFire™ Design Suite is a Graphical User Interface (GUI) tool using Data Flow Methodology which combines Annapolis's extensive systems and application development experience with their large collection of tightly crafted high performance Intellectual Property (IP) Cores, the automatic generation of the logic necessary to control the interfaces between the modules, and Hardware in the Loop Debugging to provide an exceedingly convenient and fast methodology for developing FPGA application files. With CoreFire™ it is possible to completely implement an algorithm on our WILD™ Family of Field Programmable Gate Array (FPGA) boards without ever descending to the lower level hardware details, saving months of development time and money.

FPGA designers who have struggled for months to develop applications using VHDL are finding that CoreFire™ enables them to achieve better FPGA performance in a fraction of the time.

Combined with the Annapolis COTS WILDSTAR™ 4 / 5 / 6 FPGA boards with many million gates in each slot, using Xilinx Virtex™ 4, 5 and 6, the power of CoreFire™ can automatically and quickly provide correct, reconfigurable and reliable FPGA designs for these boards. Real world application experience has shown CoreFire™ to be the critical tool that enables the timely development of highly specialized FPGA designs, ensuring each program's success.

Gone are the days when an Application Developer had to learn hardware design methodologies, such as VHDL, Verilog, or low level schematic entry. CoreFire™'s "drag and drop" approach keeps the User operating on the conceptual, data flow level of his problem throughout the whole development process so he can concentrate on solving problems, not on designing hardware.



WILDSTAR 6
VHDL HW Interfaces
(Full Source Code Provided)

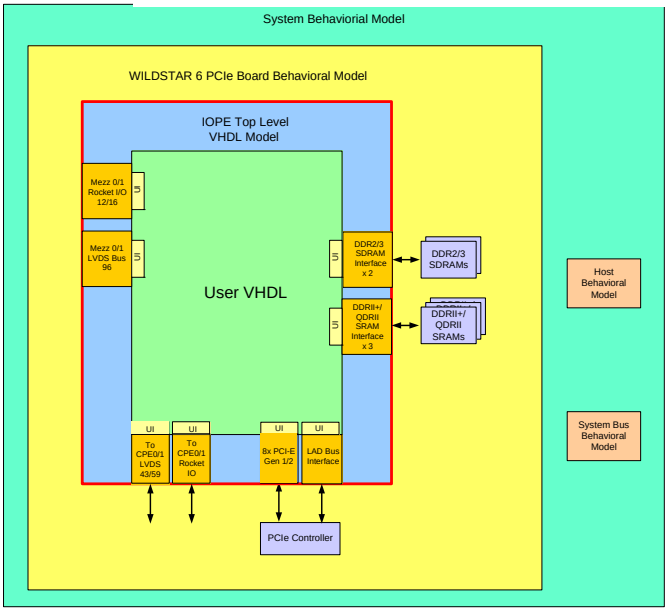
- LAD Bus
- DMA Bus
- DDR2 and DDR3 SDRAM
- DDRII+/QDRII+ SRAM
- Rocket I/O Mezzanine Interface
- LVDS I/O Mezzanine Interface
- Interfaces between FPGAs
- High Speed Rocket I/O to Backplane
- Basic Board Functions - Clocks, Reset, LEDs

WILDSTAR 6
VHDL IO Communication Interfaces
(Encrypted Cores Provided)

- 1 GbE
- 8x PCI-E Gen 1 and Gen 2

FPGA VHDL Template

- User VHDL is instantiated into the provided PE top level VHDL model
- User manually includes the supplied Annapolis physical interfaces
- User writes VHDL code to interface to the Annapolis interfaces



Abstract Chip Level Interfaces

- Physical pad locations are available and accessible by the developer, but are abstracted within the VHDL model for ease of use
- Abstract tri-state control of bidirectional buses
- Simplify multi-cycle interfaces to single cycle operations
- De-multiplex multiplexed bus interfaces
- Optimized clocking scheme

WILDSTAR 6 Host Software

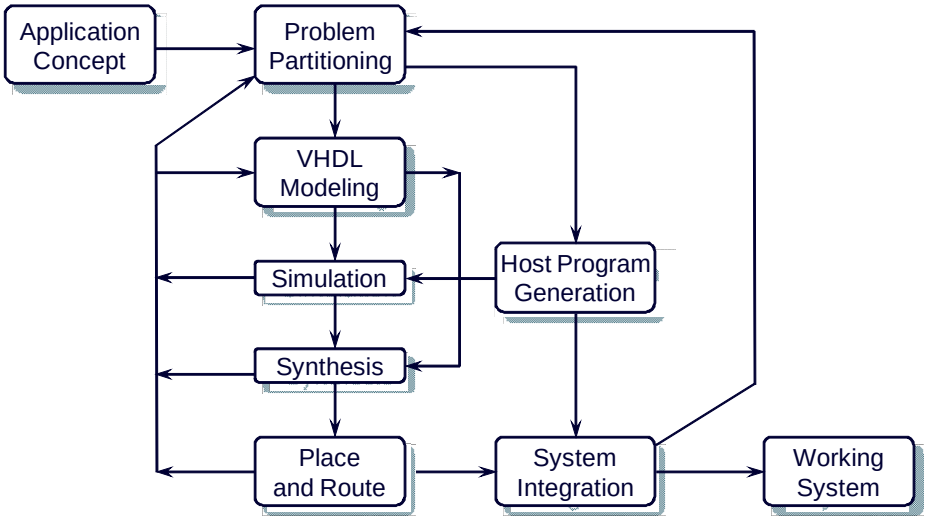
- Allows Host System access to the WILDSTAR 6 Board
- C API Function Calls to interact with System
- C API Function Calls to Configure Board
- C API Function Calls to Transfer Data

Driver API Function Call Modules

- Clock - Provides access to WILDSTAR 6 clocks
- Direct Memory Access (DMA) - Provides interface between the PEs and the PCIe Cntroller
- Error - Monitors and queries API errors
- General - Allows a WILDSTAR 6 board to be detected and initialized
- Information Access - Provides access to information from various sources
- Interrupt Handling - Provides access to Interrupts and Interrupt Handling
- Processing Element (PE) - Provides interface to configure and program WILDSTAR 6 PE
- Register Access - Provides access to the register space of WILDSTAR 6 PE
- Sensor - Provides access to board sensors
- XML Description - Allow direct access to hardware descriptions in XML format
- API Function Calls to Configure Board
- Monitor and Control On Board Temperature and Power

WILDSTAR 6 VHDL Support Tools

- Simulation - Mentor Graphics ModelSim
- Synthesis - Synplicity Synplify Xilinx XST
- Place and Route - Xilinx



Annapolis VHDL Hardware Interface Models

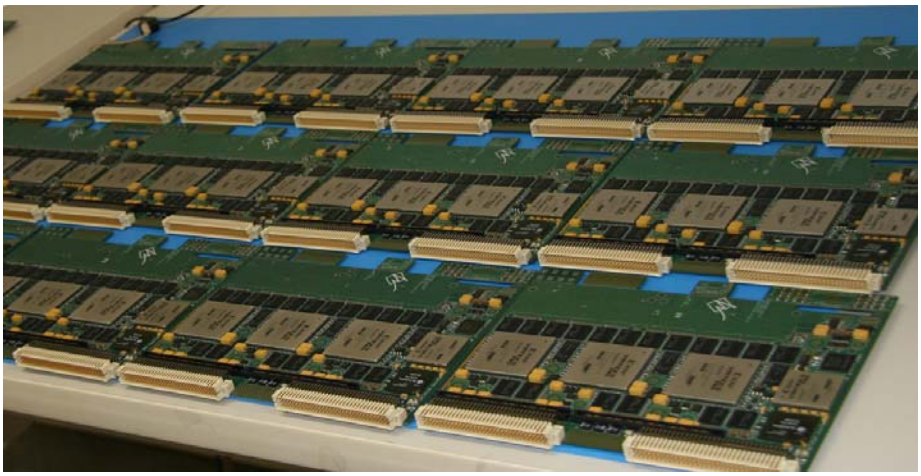
- Optimized for best performance and lowest latency.
- Provide fully tested interfaces to drastically reduce customer design iterations
- Full open source, for maximum visibility and access by the developer

WILDSTAR 6 VHDL Design Methodology

- Write VHDL user code for PE using provided template
- Connect VHDL user code up to provided user interfaces (LAD bus, DMA, DRAM, etc.)
- Simulate design using included ModelSim scripts and verify its functionality using VHDL "host code" templates to simulate software API calls
- Synthesize design with Synplify or XST using included script files
- Place and Route design using Xilinx tools using included script files
- Write C code using provided templates to program in compiled PE image and run applicable API calls
- Run the completed FPGA file on the WILDSTAR 6 hardware and the compiled C code on the onboard Host PPC

VHDL Model Simulation Environment

- Behavioral Model of all functional components on WILDSTAR 6 PCIe
- Synthesizeable Source VHDL of hardware interfaces to all PE accessible components (LAD Bus, DMA, DRAM, etc)
- Individual Source Examples for each hardware interface
- Scripts for simulation, synthesis, and place & route
- Templates for user to develop VHDL PE designs
- Documentation on all of the above
- Support for Mentor Graphics ModelSim, Synplicity Synplify, Xilinx XST, and Xilinx ISE Foundation tools
- Support for Xilinx ChipScope
- System Level Model
  - Simulate the Host Computer, Place Multiple Boards in a System, and arbitrarily interconnect the Boards to each other and to External Sources
- Board Level Model
  - Simulate Board Components - Memories, Buses, I/O Ports
- PE Level Model
  - PE Interfaces and User Logic for driving PE pins
  - Completely synthesizable
- Will eventually become the Bitstream that programs the PE



In House Manufacturing

Annapolis has been building and delivering COTS and Custom Software, Hardware and System Products for Fortune 100, Fortune 500 and Government Customers since 1982. We know how to manufacture state of the art high performance boards, and have many years experience successfully producing surface mount products.

The Annapolis Engineering Team has many many years of experience working on the cutting edge of technology.

Proactive Thermal and Power Management To Ensure Safe and Reliable Processing

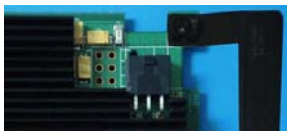
- Combination Heat Sink/Fans
- Sensors across the board monitor Current, Voltage and Temperature, with automatic warning/shutdown capability to prevent excessive heat buildup
- Individual Power Supply and Management for each I/O Slot and each FPGA Processing Element
- All monitoring and control through Host Software via API Calls
- Replaceable Fans have a Monitor Sense Line

Sample WILDSTAR 6 PCIe Part Number

WS6/XC6LX240T-2E/XC6SX240T-2/2.6GD2D/1GD2D/PWB
Board Family, # CPEs & Temperature Range /
CPE FPGA Type -Speed Grade & Backplane Type /IO FPGA Type -Speed Grade /
Total CPE Memory / Total IOPE Memory / IRIG-B Option / Conformal Coating

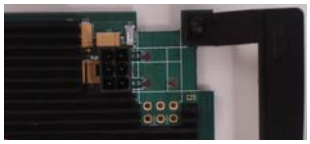
WILDSTAR™ 6 for PCI Express Part Number

WS6/ = WILDSTAR™ 6 with 2 Computational Processing (CPE) FPGAs (Default)
or WS61 = WILDSTAR™ 6 with 1 CPE FPGA
or WS6Ind/ = WILDSTAR™ 6 Industrial Temperature Range with 2 CPE FPGAs
or WS61/Ind = WILDSTAR™ 6 Industrial Temperature Range with 1 CPE FPGAs
XC6xxxxxx = Virtex 6 FPGA Computational Processing Element:
LX240T, LX365T, LX550T, SX315T, SX475T
or B- = I/O FPGAs only, no Computation FPGAs
-x = Speed Grade: -1 = 1C or 1I, -2 = 2C or 2I, -3 = 3C
x/ = Backplane: E = PCI Express
XCxxxxxx = Virtex 6 FPGA IO Processing Element:
LX240T, LX365T, LX550T, SX315T, SX475T
-x = Speed Grade: -1 = 1C or 1I, -2 = 2C or 2I, -3 = 3C
/xxxx = CPE FPGA Memory:
For LX240T, LX365T and SX315T = 640MD2D, 1.3GD2D, 2.6GD2D, 5.2GD2D, 1.3GD3D, 2.6GD3D, 5.2GD3D, 20 MD2+S, 40MD2+S, 80MD2+S, 160MD2+S, 320MD2+S, 20MQ2S, 40MQ2S, 80MQ2S, 160MQ2S and 320MQ2S
For LX550T and SX475T = 768MD2D, 1.5GD2D, 3GD2D, 6GD2D, 1.5GD3D, 3GD3D, 6GD3D, 24MD2+S, 48MD2+S, 96MD2+S, 192MD2+S, 384MD2+S, 24MQ2S, 48MQ2S, 96MQ2S, 192MQ2S AND 384MQ2S
D2D = DDR2 DRAM, D3D = DDR3 DRAM, D2+S = DDRII+ SRAM, Q2S = QDRII SRAM,
/xxxx = I/O PE FPGA Memory:
512MD2D, 1GD2D, 2GD2D, 1GD3D, 2GD3D,
12 MD2+S, 24MD2+S, 48MD2+S, 96MD2+S, 12MQ2S, 24MQ2S, 48MQ2S, 96MQ2S
/PWx = Orientation of External Power Connector
PWT = Parallel to Board and Facing Top of Board
PWB = Parallel to Board and Facing Back
PWP = Perpendicular to Board
/IRIGB = Add IRIG-B Option
/CC = Conformal Coating



PWT

PWB



PWP